

**ECE 448**  
**Midterm Exam 1**  
**Monday, March 3, 2008**

**Problem 1 (2.5 points)**

For a given below VHDL code, provide solutions to the following problems:

1. Which type of a finite state machine, Moore or Mealy, does this code implement?
2. Draw an **ASM chart** describing this FSM. Assume that all inputs and outputs are active with logic one.
3. Supplement timing waveforms given in the answer sheet with values of **State** and output **y**.

```
library IEEE;
use IEEE.std_logic_1164.all;
```

```
entity PROBLEM1 is
port (
  CLK: in STD_LOGIC;
  Reset: in STD_LOGIC;
  a: in STD_LOGIC;
  b: in STD_LOGIC;
  y: out STD_LOGIC);
end;
```

```
architecture PROBLEM1_arch of PROBLEM1 is
  type SType is (S0, S1, S2, S3);
  signal State: SType;
begin
  State_machine: process (CLK)
  Begin
    if Reset = '1' then
      State <= S0;
    elsif CLK'event and CLK = '1' then
      case State is
        when S0 =>
          if a='1' then
            State <= S2;
          elsif b= '1' then
            State <= S1;
          else
            State <= S0;
          end if;
        when S1 =>
          if b='0' then
            State <= S0;
          elsif a= '1' then
            State <= S3;
          end if;
      end case;
    end if;
  end process;
end PROBLEM1_arch;
```

```

        else
            State <= S2;
        end if;
    when S2 =>
        if a='0' then
            State <= S3;
        else
            State <= S2;
        end if;
    when S3 =>
        if a='1' AND b='1' then
            State <= S3;
        else
            State <= S0;
        end if;
    when others =>
        null;
    end case;

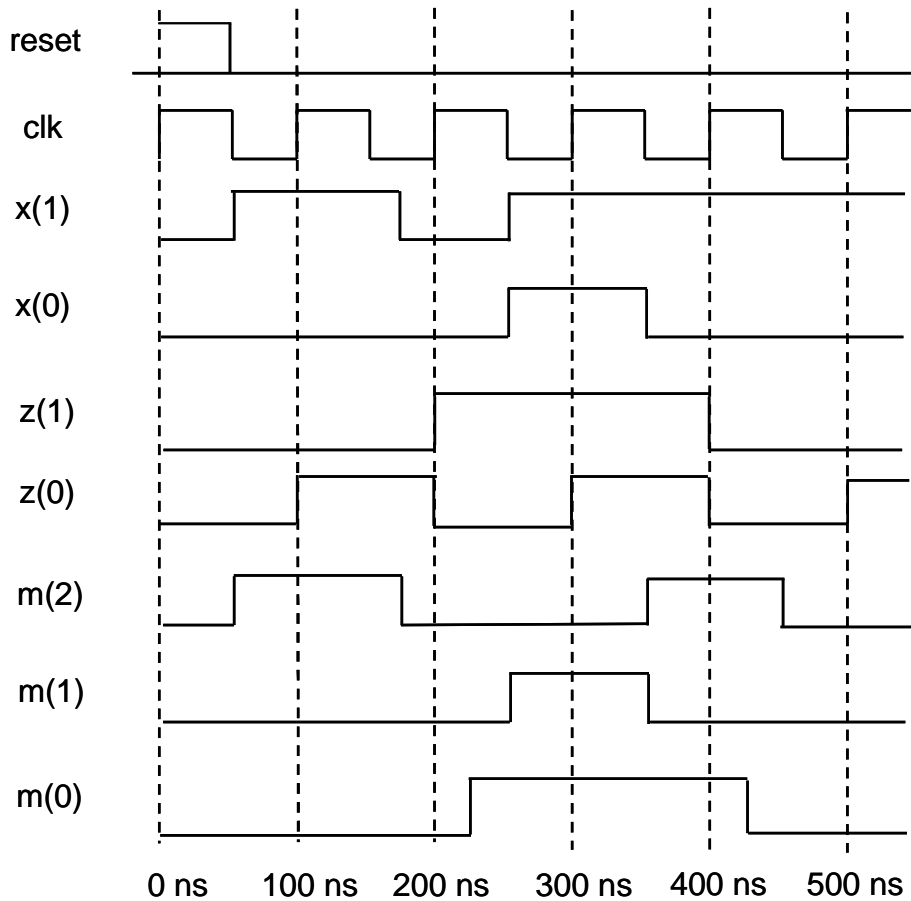
end if;
end process;

y_assignment:
    y <= '1' when (State = S2 OR State = S3) else
        '0';
end PROBLEM1_arch;

```

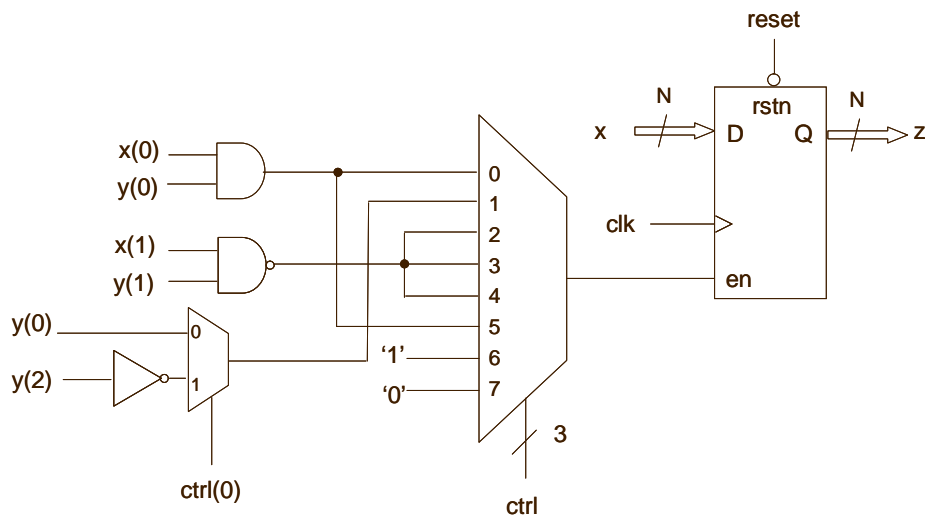
**Problem 2 (2.5 points)**

Write a testbench that generates the following input stimuli. Assume that the signals `clk` and `z` are periodical, and the signals `reset`, `m` and `x` are non-periodical. Do your best to minimize the amount of lines of VHDL code you write, e.g., by employing VHDL instructions such as `FOR LOOP`, etc.



### Problem 3 (2.5 points)

Describe the following digital circuit in synthesizable VHDL using a minimum number of (preferably only two) concurrent statements and one process. You need to provide both entity architecture, and entity declaration. Assume that the reset input of the register is synchronous, and the size of the data bus,  $N$ , is provided as a generic.



### Problem 4 (2.5 points)

What is a minimum number of Spartan 3 Logic Cells (one Logic Cell =  $\frac{1}{2}$  of a CLB Slice) necessary to implement

- 56-bit register with a serial input, serial output, and reset
- Functions  $y_1 = x_1x_4 + x_2x_3 + x_3x_5$ ,  $y_2 = x_1x_2x_5 + x_1x_3 + x_1x_5$
- 32-bit ripple-carry adder
- 40-bit shift register with serial input and parallel output
- Four-input priority encoder
- 256x8 single-port RAM
- 64x16 dual-port RAM
- 4-bit register with a serial input, serial output, and enable

Which components of Logic Cells (Multipurpose LUT, Carry & Control, Storage Element) are used in each case, and in which mode of operation (ROM, RAM, shift-register, fast carry logic, latch, flip-flop, etc.) they work?