Answers

Task 3

A_reg:

Number of Logic Cells: 4
Part of a Logic Cell: MLUT C&C SE
Mode of MLUT (for MLUTs only) ROM RAM SR

B_reg:

Number of Logic Cells: 4
Part of a Logic Cell: MLUT C&C SE
Mode of MLUT (for MLUTs only) ROM RAM SR

Single FF:

Number of Logic Cells: 1
Part of a Logic Cell: MLUT C&C SE
Mode of MLUT (for MLUTs only) ROM RAM SR

Single FA:

Number of Logic Cells: 1
Part of a Logic Cell: MLUT C&C SE
Mode of MLUT (for MLUTs only) ROM RAM SR

or

Number of Logic Cells: 2
Part of a Logic Cell: MLUT C&C SE
Mode of MLUT (for MLUTs only) ROM RAM SR

Single HA:

Number of Logic Cells: 1
Part of a Logic Cell: MLUT C&C SE
Mode of MLUT (for MLUTs only) ROM RAM SR

or

Number of Logic Cells: 2
Part of a Logic Cell: MLUT C&C SE
Mode of MLUT (for MLUTs only) ROM RAM SR
Single AND

Number of Logic Cells: 1
Part of a Logic Cell: MLUT C&C SE
Mode of MLUT (for MLUTs only) ROM RAM SR

Total number of Logic Cells: \(4+4+5+1+3+5 = 22\)
Total number of CLB slices: 11

What other component of the Spartan 3 FPGAs could be used to perform the same operation?

Dedicated multiplier

What would be the difference in the operation of these two alternative implementations in terms of:

1. number of clock cycles

   8 clock cycles for the bit serial multiplier,
   1 clock cycle for the dedicated multiplier

2. use of CLB slices

   11 CLB slices for the bit serial multiplier
   0  CLB slices for the dedicated multiplier.

3. dependence between the amount of resources used and the width of operands, k, for \(2 \leq k \leq 16\).

   proportional to k for the bit serial multiplier,
   independent of k for the dedicated multiplier.