ECE 448: FPGA and ASIC Design with VHDL

Spring 2009

Lab Syllabus

Tuesdays 7:20 –10:00pm
Section 201 (CRN: 14299)
Ekawat "Ice" Homsirikamol
ehomsiri (at) gmu.edu

Wednesdays 7:20 –10:00pm
Section 203 (CRN: 14302)
Marcin Rogawski
mrogawsk (at) gmu.edu

Thursdays 7:20 –10:00pm
Section 202 (CRN: 14301)
Marcin Rogawski
mrogawsk (at) gmu.edu

Office Hours:
Ekawat "Ice" Homsirikamol Mondays 5:30-7:00 PM
Marcin Rogawski Tuesdays 1:00-2:30 PM
Marcin Rogawski Wednesdays 1:00-2:30 PM

Other days and times by appointment

Location:
All lab sections and office hours will be held in the Computer Engineering Lab, S&T 2, room 203.

Lab Description:
The lab sections allow students to learn tools and methodologies used to develop complex digital systems using FPGAs. The designs will be first verified using functional, post-synthesis and timing simulation, and then experimentally tested using prototype FPGA boards. For each lab assignment, students are expected to submit a set of deliverables listed in the text of each experiment.

Required Hardware:
Majority of experiments will be implemented using Celoxica RC 10 FPGA Boards. Students are not required to purchase any boards or other equipment used in the labs. The boards will be provided to the students during the lab sessions, office hours, and on-demand by checking out the boards from the research lab located in S&T 2, room 220, and/or Dr. Gaj's office, S&T 2, room 223.

Grading:
Lab Experiments: 40% of points for the entire class
Midterm Exam for the Lab: 15% of points for the entire class
General Laboratory Rules:

- Each lab experiment will be preceded by an introduction and a hands-on session taught by a TA.
- The deadlines for submitting all experiment deliverables (including source codes, diagrams, waveforms, configuration files, etc.) are being set as follows:
  - Tuesday section - Tuesday, 7:00 PM
  - Wednesday section - Wednesday, 7:00 PM
  - Thursday section - Thursday, 7:00 PM.
- Students will be required to demonstrate working experiment during a lab session on a day designated as a due date for a particular lab experiment.
- Experiment demonstrations will be accepted exclusively during the class time for a particular lab section.
- For each experiment, the demonstration and the electronic deliverables (including lab report) are each worth 50% of points allocated to a given experiment.
- Each lab experiment that is late will be penalized by deducting 1/3 of its allocated points per number of weeks that is late. As a result, no credit will be received for a lab experiment that is more than two weeks late. The additional opportunities will be provided to earn bonus points by completing additional requirements for each experiment or by completing experiment a week or more ahead of schedule. Both penalty and bonus points will apply independently to the demonstrations and to the electronic deliverables.
- Office hours will be devoted to helping students with their experiments and answering any questions related to the subject of the course.
- Students are required to work individually on all experiments from Part I of the course, and either individually or in groups of two students on all experiments from Part II of the course. In case of the group work, both students are expected to be intimately familiar with the entire solution to the given experiment and the entire experiment report. This knowledge will be verified during the experiment demonstration and the same grade will be applied to the entire team.
- Every completed experiment must be presented to your TA, who will evaluate students' results and effort. It is the students' responsibility to convince the TA that their designs work as required. Therefore, students have to simulate and test their designs thoroughly and well document their work. The TA is not required to test anything by himself nor to investigate if the designs are correct in case of insufficient documentation.
- In order to prevent cheating and plagiarism, the students will be required to
  - submit all electronic deliverables using Blackboard at the designated time before the experiment demonstration,
  - restrain from any changes in the experiment files in the period between the electronic submission and the experiment demonstration,
  - answer correctly several detailed questions regarding their experiment solution at the time of demonstration.
Not complying with either of these requirements may lead to either a total rejection of the demonstration by the TA, or to a substantial reduction of the number of points awarded to the student.
• In case of any evident attempt to submit somebody else’s work as your own, both
students involved in the incident may be penalized by taking away all points for
the given experiment. The two repeated attempts to present somebody else’s work
as your own may lead to the F grade for the entire course, independently of the
total amount of points earned by the student before the second incident.

• The students are encouraged to help and support each other in all problems related
to the
- operation of the CAD tools,
- operation of the FPGA boards,
- operation of the measurement equipment available in the lab,
- understanding of the problem to be solved during each experiment.

**Tentative schedule of the labs (subject to possible modifications):**

1. Implementing combinational logic in VHDL. Aldec Active-HDL.

2. Implementing sequential logic in VHDL. ModelSim.

3. Implementing digital systems using FPGAs. Post-synthesis & timing
   simulation, experimental verification with the FPGA board. Synplicity
   Synplify Pro and Xilinx Implementation Tools called from Active-HDL.

4. Implementing digital systems based on finite state machines. Xilinx XST
   and Xilinx Implementation Tools called from Xilinx ISE.

5. Review before the Midterm Exam for the Lab.
   February 24-26, 2009

6. Midterm Exam for the Lab.
   March 3-5, 2009

7. Implementing complex digital systems divided into datapath and

8. Implementing complex digital systems including memory. Advanced
   testbenches.

9. Implementing and testing complex digital systems based on embedded
   microprocessors. Testing digital systems using logic analyzer.