Midterm Exam 2 Specification

Resources

68HC11 E-series Reference Guide
and if necessary
    68HC11 E-series Technical Data
    68HC11 Reference Manual
all available at
        http://www.technologicalarts.com/myfiles/links.html

Optionally:
Peter Spasov, *Microcontroller Technology*,
any edition, Prentice-Hall, Chapter 2, Software,
and Chapter 7 Clocked Operation
(you can borrow this book from the ECE 447 students).

Microcontroller

Using high-level behavioral VHDL describe an 8-bit microcontroller **MC68HC11E1**, working in the ***expanded mode***, with the following simplifications:

1. Inputs and outputs of the microcontroller are reduced to E (clock), RESETn (reset active low), RW (read/write), AS (address strobe), ADDR15..8 (also denoted as PB7..0), ADDR7..0/DATA7..0 (multiplexed address & data, also denoted as PC7..0), and PORTE.

2. Internal registers are reduced to the registers
   B, IY, SP, CC (Condition Codes NZVC), and PC.

3. The only parts of 68HC11E1 implemented in your model are:
   a. CPU
   b. RAM (256 B in the range $1800-$18FF)
   c. parallel I/O (PORTE)

4. Internally generated clock E has a frequency 2 MHz.

5. Internal I/O registers are limited to
   PORTE at the memory address $100A

6. Instruction set of the microcontroller is reduced to the following instructions

a. Data transfer instructions
   LDAB, LDY, STAB
b. Arithmetic instructions
   NEGB, ADDB, ASRB
c. Logic instructions
   EORB
d. Data test instructions
   BITB
e. Control instructions
   BEQ, JSR
f. Stack instructions
   PSHA, PULY

7. Addressing modes of the microcontroller are reduced to the following modes
    a. immediate
    b. indexed
    c. inherent
    d. relative

8. Main program is stored in the *external* RAM starting at the address $0000.

9. After reset, PC is set to the address $0000

Microcontroller system

The implemented microcontroller system should consist of:

1. Microcontroller MC68HC11E1
2. 8 kB RAM, such as 6164
3. 74HC373 8-bit latch
4. 74HC138 decoder chip
5. Auxiliary gates, if needed

Features of the model

1. Your model should allow cycle accurate modeling
   of the circuit behavior.
2. Your model should contain debugging features
   similar to the debugging features of the DLX model,
   discussed in class and described in Ashenden, Chapter 15.
3. Generic parameters passed to the model
   should include
   a. name of the file with the contents of the external RAM
   b. clk-to-output delay
   c. debugging mode
4. Your model should report all undefined opcodes,
   treat them as NOP, and proceed to the next RAM address.

Testing and debugging

The behavior of your model should be carefully verified using a testbench instantiating your model with

a. the external RAM containing a valid program composed of a substantial subset of instructions implemented in the model

b. debugging mode set to the most detailed mode (trace_each_step)

Deliverables

1. All source code files.
2. Contents of the external RAM used for the model verification, in the hexadecimal notation, and expressed using the corresponding 68HC11 assembly language mnemonics.
3. The detailed log/report generated by your model for a given contents of RAM, and with the debugging mode set to trace_each_step.