Status registers used for communication between two FSMs.
Set by one FSM & reset by another FSM.
All set & reset signals are synchronous.
Set signal has a higher priority.
Set & clr should not be active simultaneously during normal operation.

Set or clr signal comes from an FSM driven by a slower clock.
This signal must be gated by the signal
last/fast_clk_cycle, which is active only during the last clock cycle of a faster clock before the rising edge of a slower clock.
This signal is generated by the following circuit: