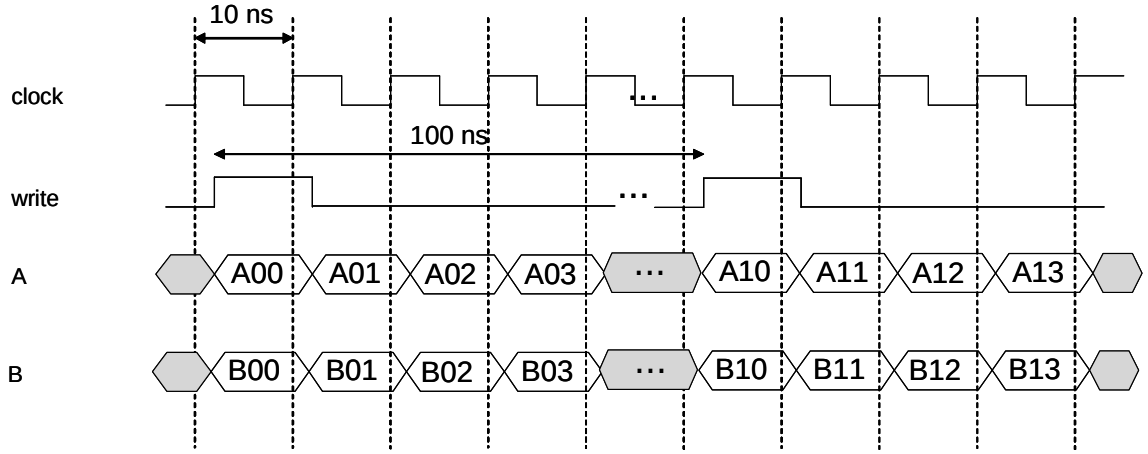
ECE 545: Fall 2005
Midterm Exam 1

Problem 1 (10 points)

Function

Draw a block diagram and an ASM chart describing a digital circuit capable of executing the following function:

The circuit accepts samples from two A/D converters, provided at the inputs A and B, respectively, as w-bit signed numbers in the two's complement representation. The samples are generated by each A/D converters in the groups of four, separated by 10 ns within each group, as shown in the figure below. Two consecutive groups of samples are separated by 100 ns. The circuit should compute an average value of four samples within each group, and then compare an average for a group entered using input A with an average for a group entered using input B. A special counter, initialized to zero using reset at the beginning of processing, should be incremented each time an A average is greater than the B average, and decremented in the opposite case. If both averages are the same, the counter should remain unchanged. When the counter reaches a threshold of +10, it does not increment any longer, and it generates an active value at the output *overflow*, each time A average is greater than the B average. Similarly, when the counter reaches value -10, it does not decrement any longer, and it generates an active value at the output *underflow*, each time A average is smaller than the B average. Values of the counter, and the signals *overflow* and *underflow* should remain unchanged in the period between two consecutive comparisons. A new value of the counter should be indicated with the output control signal *new_count*, which should be set to high for <u>two</u> clock cycles after the computation of the new value of the counter, and set to zero otherwise.



In your block diagram mark clearly the sizes of all buses. Write VHDL code ONLY for basic components used in your block diagram.

Optimization

Design your circuit for the <u>minimum total execution time</u>. When choosing between two circuits with the same or very similar execution time, give preference to the circuit with the smaller area.

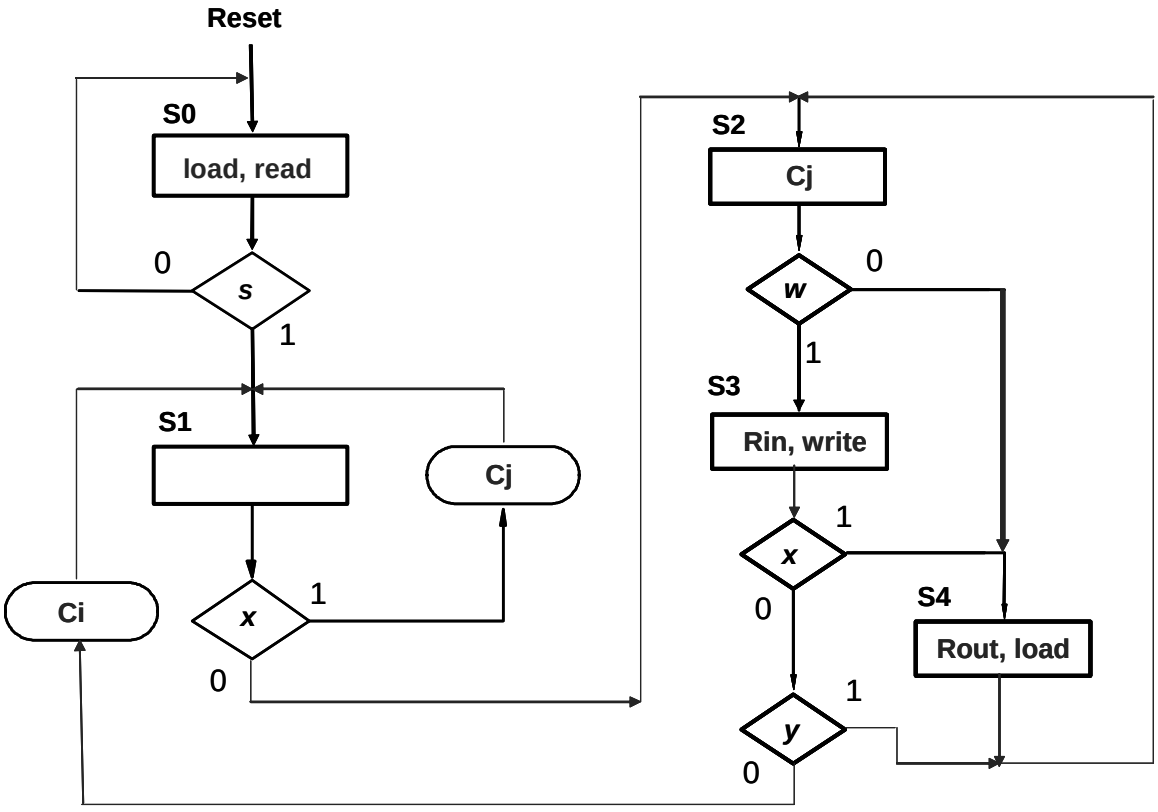
Interface

Assume the following interface to your circuit:

Port	Width	Meaning
Inputs		
clk	1	System clock
reset	1	System reset – clears internal registers
A	w	Input A for samples produced by the first A/D converter
B	w	Input B for samples produced by the second A/D converter
write	1	Signal set to high when the first sample of each group of four is present at the inputs A and B
Outputs		
count	4	Value of the special counter
overflow	1	Indication of an overflow
underflow	1	Indication of an underflow
new_count	1	Set to HIGH for two clock cycles, after a new value of count is computed

Problem 2 (5 points)

Translate the given below ASM chart to the corresponding synthesizable VHDL code:



Problem 3 (5 points)

Translate the given below block diagrams to the corresponding synthesizable VHDL code: