ECE 545: Fall 2006
Midterm Exam 1

Problem 1 (10 points)

Function

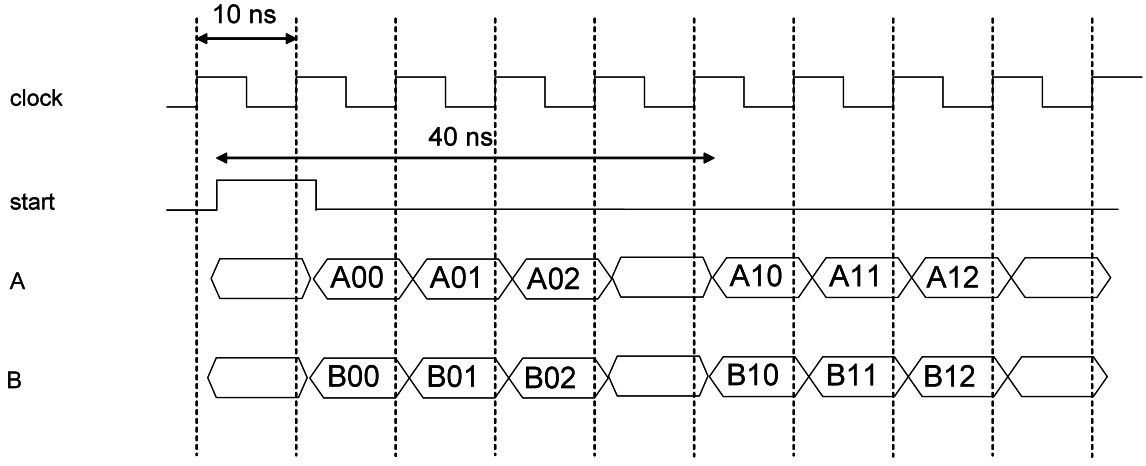
Draw a block diagram and an ASM chart describing a digital circuit capable of executing function described below. In your block diagram mark clearly the sizes of all buses, and the critical path. Your circuit should be optimized for minimum clock period and the minimum amount of internal memory. In particular, the circuit must not store input data before processing.

The circuit accepts samples from two A/D converters, provided at the inputs A and B, respectively, as w-bit signed numbers in the two's complement representation. The samples are generated by each A/D converter in the groups of ***three***, separated by 10 ns within each group, as shown in the figure below. Two consecutive groups of samples are separated by 40 ns. The first sample of the first group is preceded by an active value of the input *start*.

The circuit should compute a ***median*** value of three samples within each group, and then compare a median for a group entered using input A with a median for a group entered using input B.

The larger of the two medians should be stored in an internal memory of the size of 512 2^w words for further processing. If the medians are equal, none of them gets stored, but the counter called *equal_counter* is incremented. When the internal memory gets full, an output called *full* should be activated. At this point, an external circuit should be able to read data from the internal memory word by word, starting from the location 0, using *read* as a control signal. After all data are read, the circuit activates signal *done*, waits for an active value of the signal *start*, resets *equal_counter* and *done* and repeats the operation described above.

Hints: The ***median*** of a population is the point that divides the distribution of scores in half. Numerically, half of the scores in a population will have values that are equal to or larger than the median and half will have values that are equal to or smaller than the median. *Please note that a median of a group of three values is the second largest value in the group.*



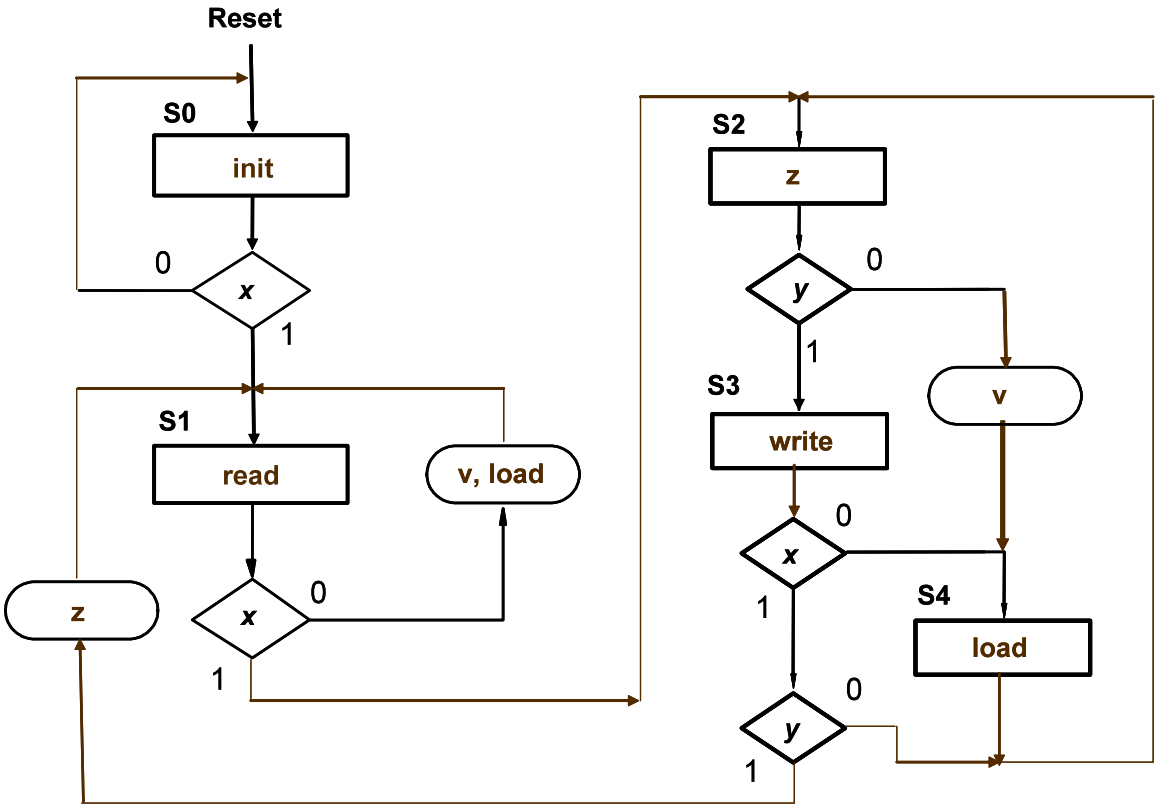
Interface

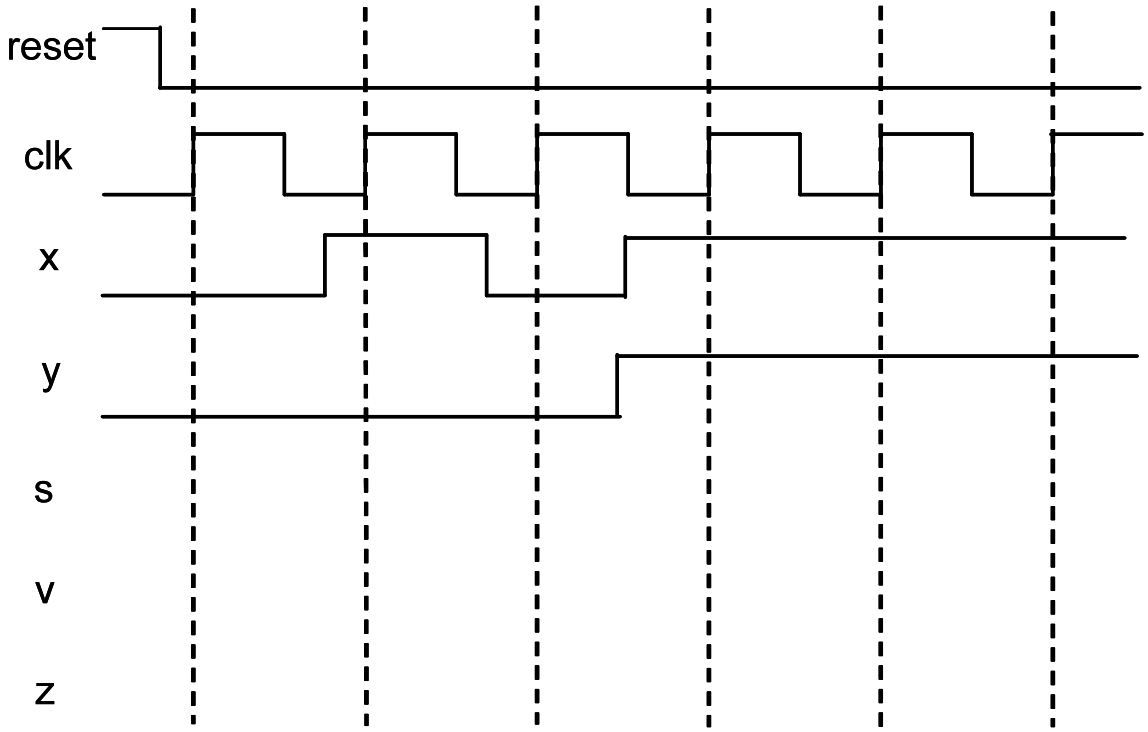
Assume the following interface to your circuit:

Port	Width	Meaning
Inputs		
clk	1	System clock
reset	1	System reset – clears internal registers
A	w	Input A for samples produced by the first A/D converter
B	w	Input B for samples produced by the second A/D converter
start	1	Signal set to high one clock cycle before the first sample of the first group arrives at the inputs A and B
read	1	Control signal used to read data word by word from the internal memory
Outputs		
data_out	w	Data output for reading data out from the internal memory
equal_counter	10	Value of the *equal_counter*
full	1	Internal memory full
done	1	All data read from the internal memory

Problem 2 (5 points)

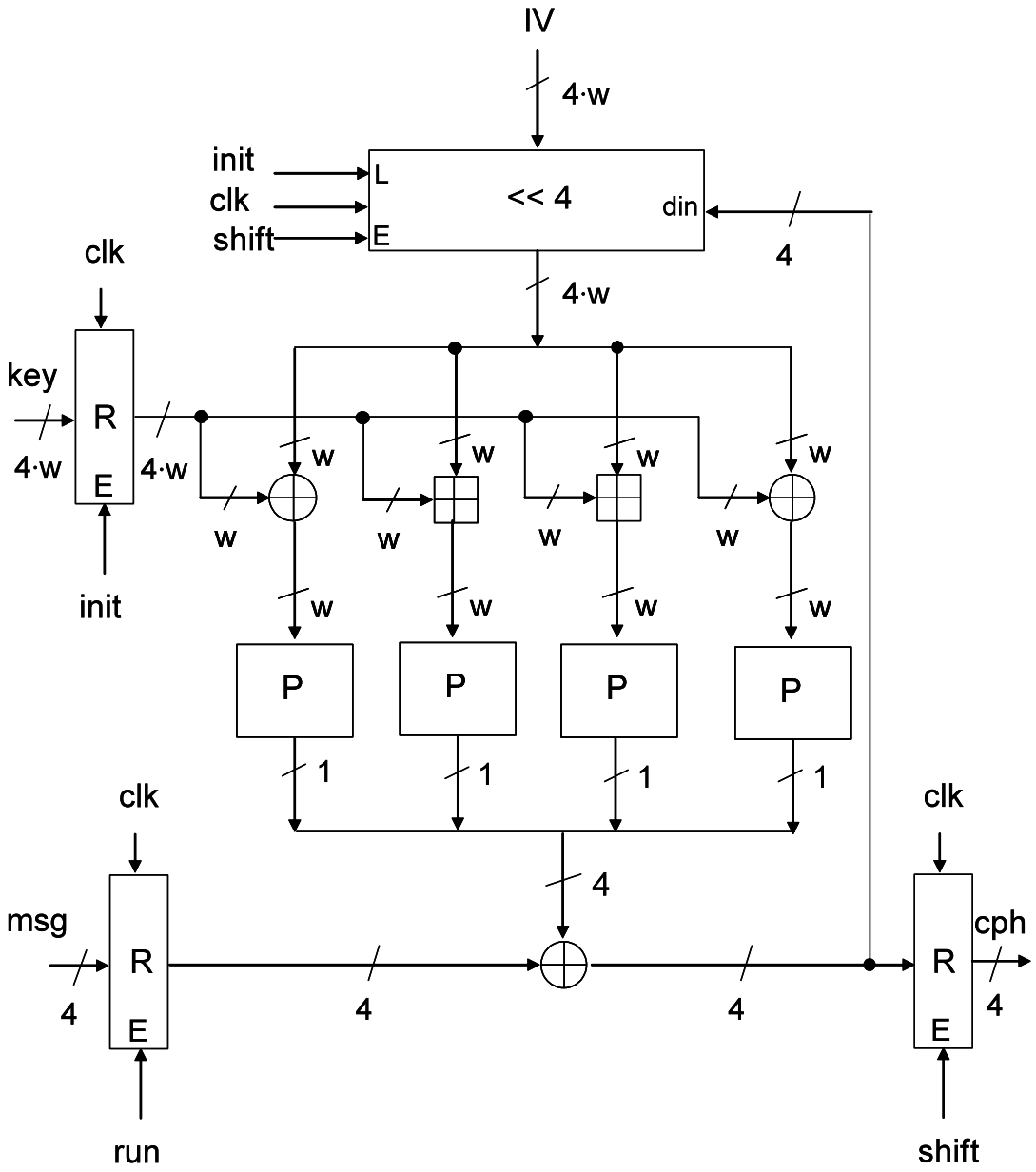
Translate a given below ASM chart to the corresponding synthesizable VHDL code, and supplement given below timing waveforms with the values of the state s and outputs v and z. Provide both design architecture and design entity.





Problem 3 (5 points)

Translate a given below block diagram to the corresponding synthesizable VHDL code. Provide design architecture only (both declarative and functional part), you do not need to provide design entity.



Notation:

⊕ denotes bitwise XOR

⊞ denotes unsigned addition modulo 2^w

P denotes odd parity generator, i.e., the circuit that generates 1 when an odd number of its inputs is equal to 1

R represents a register with an enable input E

<< 4 represents a shift register with a parallel load signal L, enable signal E, and a digit-serial input din.