ECE 545 Final Exam

Device family: Spartan 3
Device: 3s50pq208-4
Xilinx XST: ISE Webpack 9.1

Synthesis

Synthesized with 5 warnings, all ignored. 3 of the warnings were for unused bits in data buses. This was intentionally done as a way to do modulo. The last 2 warnings were for use_dsp48 not being applicable for the used technology.

Results:

Number of Slices: 105 out of 768 13%
Number of Slice Flip Flops: 109 out of 1536 7%
Number of 4 input LUTs: 173 out of 1536 11%
Number of IOs: 70
Number of bonded IOBs: 70 out of 124 56%
Number of MULT18X18s: 4 out of 4 100%
Number of GCLKs: 1 out of 8 12%
Minimum Clock period: 19.106ns
Maximum frequency: 52.341MHz

Implementation

Implementation completed with 0 error and 0 warnings:

Results:

Minimum Clock period: 20.910ns
Maximum frequency: 47.824MHz