Project Deliverables
Deliverables Common for All Students

1. Detailed block diagrams of the Datapath with names of intermediate signals matching VHDL code [electronic version in Xfig and PDF]

2. Interface with the division into the Datapath and the Controller [electronic version in Xfig/PPT, and PDF]

3. ASM charts of the Controller, and a block diagram of connections among FSMs (if more than one used) [scanned handwritten version OK, electronic version in Visio/Xfig a bonus]

4. RTL VHDL code of the Datapath, the Controller, and the Top-Level Circuit
Deliverables (2)

5. Verification

A. All testbenches used to verify circuit operation at various levels of the hierarchy.
B. All test vector files you have used in your simulations.
C. Short report describing:
   - your strategy for verification: order of tests and testbenches used,
     source of test vectors
   – highest level entity verified for functional correctness and the results of its verification for
     * post-synthesis simulation (one family)
     * timing simulation (one family)
   – verification of lower-level entities

6. Updated timing analysis (execution time and throughput); formulas for timing confirmed through simulation!
Deliverables (3)

7. Critical Path

A. The file
critical_path.pdf
describing your efforts on identifying and minimizing the critical path in your circuit.
B. Graphical view of your final critical path obtained using Synplify Premier DP.
C. Textual description of your final critical path, obtained from the static timing analysis report.
D. Your hierarchical block diagram (from 1_block_diagrams) with the critical path marked in red.
Deliverables (4)

8. Report on benchmarking using ATHENa

– Two Xilinx families
– Two Altera families
– Optimization strategies used to obtain best results
  single_run (minimum), other ATHENa optimizations (bonus)
– Graphs and charts
– Observations and conclusions
Deliverable for Students Working on Pipelined Architectures

0. **analysis leading to the choice of a particular pipelined architecture as the most efficient architecture in terms of the throughput to area ratio.**

If your analysis was supported by a full or partial implementation of any alternative architectures, please include the corresponding block diagrams, interface, ASM charts, etc. in the subsequent directories, and only refer to them in your report analysis.pdf.
Bonus Deliverables

Bugs and inefficiencies found in

– ATHENa
– GMU CERG Source Codes
– Block diagrams
– Discrepancies between source codes and Block diagrams
– Other