Homework 1  
due Saturday, September 13, 11:59pm  
(you can submit an electronic version using Blackboard  
 or  
the handwritten/printed version by sliding your solution under the door to my  
office; early submissions during the Thursday class on September 11 are very  
welcome)  

All solutions should be developed individually!  
The GMU Honor Code applies.

Problem 1  

A. Show how to implement an inverter using an XOR gate.  
B. Show how to implement a conditional inverter using an XOR gate.  
A conditional inverter is defined as follows:  
y = \overline{x} \text{ if } c=1; \quad y = x \text{ if } c=0.

Problem 2  
Are the following sets of gates complete sets? Are they minimal complete sets? Justify your answers.  

A. \{XNOR\}  
B. \{XOR, OR\}  
C. \{XOR, XNOR, AND\}

Problem 3  
Prove the following Boolean identities, using the truth table method:  

A. x \cdot (y + z) = x \cdot y + x \cdot z  
B. x + (y \cdot z) = (x + y) \cdot (x + z)  
C. x \cdot y + x \cdot z + \overline{y} \cdot z = x \cdot y + \overline{y} \cdot z

Problem 4  
Draw a schematic of  
A. 8-to-1 multiplexer built of 2-to-1 multiplexers  
B. 16-to-1 multiplexer built of 4-to-1 multiplexers

Problem 5  
Draw a schematic of  
A. 3-to-8 decoder with an enable input, built of 2-to-4 decoders and a minimum number of logic gates  
B. 4-to16 decoder with an enable input, built of 2-to-4 decoders and a minimum number of logic gates.
Problem 6
Show how to implement an address decoder that recognizes the following four ranges of a 16-bit address A, and generates the corresponding enable signals e0, e1, e2, e3, indicating that the address is in the given range:

Range 0: 1000-13FF
Range 1: 3000-33FF
Range 2: 5000-53FF
Range 3: 7000-73FF

All enable signals should be equal to 0, when address A does not belong to any of the above ranges.

Problem 7
Draw a schematic of an 8-to-3 priority encoder built of 2-to-1 multiplexers and a minimum number of logic gates with up to 4 inputs.

Problem 8
Show how to implement a Full Adder using two Half Adders and a minimum number of logic gates.

Problem 9
Draw a schematic of a 4-bit conditional incrementer built of Half Adders, Full Adders, and a minimum number of logic gates. A conditional incrementer is defined as follows:

\[ S = A+1 \text{ if } c=1; \quad S = A \text{ if } c=0. \]

Problem 10
Draw a schematic of a 4-bit signed number comparator performing comparison

A. A < B
B. A = B
C. A ≤ B

You can use Half Adders, Full Adders, and a minimum number of basic logic gates.

Bonus Problems

Problem 11
Show how to implement a full adder using only 2-to-1 multiplexers and 2-input XOR gates. Try to minimize the delay between cin and cout.

Problem 12
Show how to implement a variable arithmetic shifter right, C = A>>B, shifting an 8-bit input A by the number of positions given by a 3-bit input B. Hint: Use fixed shifters X>>1, X>>2, X>>4, and 2-to-1 multiplexers.