Design and implement a simple unit permitting to speed up encryption with RC5-similar cipher with fixed key set on 8031 microcontroller. Unlike in the experiment 5, this time your unit has to be able to perform an encryption algorithm by itself, executing 32 rounds......
FPGA Design process (2)

Implementation

Configuration

Timing simulation

On chip testing
Tools used in FPGA Design Flow

Functionally verified VHDL code

- Xilinx XST
- Synplify Premier
- Xilinx ISE

VHDL code

Design

Synthesis

Netlist

Implementation

Bitstream
Synthesis Tools

Xilinx XST

Synplify Premier

... and others
architecture MLU_DATAFLOW of MLU is

signal A1:STD_LOGIC;
signal B1:STD_LOGIC;
signal Y1:STD_LOGIC;
signal MUX_0, MUX_1, MUX_2, MUX_3: STD_LOGIC;

begin
  A1<=A when (NEG_A='0') else not A;
  B1<=B when (NEG_B='0') else not B;
  Y<=Y1 when (NEG_Y='0') else not Y1;

  MUX_0<=A1 and B1;
  MUX_1<=A1 or B1;
  MUX_2<=A1 xor B1;
  MUX_3<=A1 xnor B1;

  with (L1 & L0) select
    Y1<=MUX_0 when "00",
    MUX_1 when "01",
    MUX_2 when "10",
    MUX_3 when others;

end MLU_DATAFLOW;
Circuit netlist (RTL view)
Mapping
Implementation
Implementation

• After synthesis the entire implementation process is performed by FPGA vendor tools
Implementation

Writing VHDL SDF file 'time_sim.sdf' ...
INFO:NetListWriters:635 - The generated VHDL netlist contains Xilinx SIMPRIM simulation primitives and has to be used with SIMPRIM library for correct compilation and simulation.
INFO:NetListWriters - Xilinx recommends running separate simulations to check for setup by specifying the MAX field in the SDF file and for hold by specifying the MIN field in the SDF file. Please refer to Simulator documentation for more details on specifying MIN and MAX field in the SDF.
INFO:NetListWriters:665 - For more information on how to pass the SDF switches to the simulator, see your Simulator tool documentation.

Number of warnings: 0
Number of info messages: 3
Total memory usage is 186884 kilobytes

Created netgen log file 'time_sim.nlf'.
Implementation ver1->rev1: 0 error(s), 7 warning(s)
Implementation ended with warning(s).
Translation

- Circuit Netlist
- Timing Constraints
- Constraint Editor or Text Editor
- UCF
- User Constraint File
- Translation
- NGD
- Native Generic Database file

Synthesis
Mapping

Clock

LUT0

Input0
Input10

Input1
Input2

Input3
Input8
Input9

Input4
Input5
Input6

LUT1

LUT2

FF1

FF2

Output0

Input7

Output1
Placing CLB SLICES FPGA
Routing

Programmable Connections

FPGA
Configuration

• Once a design is implemented, you must create a file that the FPGA can understand
  • This file is called a bit stream: a BIT file (.bit extension)

• The BIT file can be downloaded directly to the FPGA, or can be converted into a PROM file which stores the programming information
Two main stages of the FPGA Design Flow

**Synthesis**
- **RTL Synthesis**
  - Code analysis
  - Derivation of main logic constructions
  - Technology independent optimization
  - Creation of “RTL View”
- **Map**
  - Mapping of extracted logic structures to device primitives
  - Technology dependent optimization
  - Application of “synthesis constraints”
  - Netlist generation
  - Creation of “Technology View”

**Implementation**
- Technology dependent
- **Place & Route**
  - Placement of generated netlist onto the device
  - Choosing best interconnect structure for the placed design
  - Application of “physical constraints”
- **Configure**
  - Bitstream generation
  - Burning device
## Synthesis Report Example – Resource Utilization (1)

Device utilization summary:

```
Selected Device : 6slx4tqg144-3

Slice Logic Utilization:

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Slice Registers:</td>
<td>53</td>
<td>out of</td>
<td>4800</td>
</tr>
<tr>
<td>Number of Slice LUTs:</td>
<td>163</td>
<td>out of</td>
<td>2400</td>
</tr>
<tr>
<td>Number used as Logic:</td>
<td>163</td>
<td>out of</td>
<td>2400</td>
</tr>
</tbody>
</table>

Slice Logic Distribution:

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of LUT Flip Flop pairs used:</td>
<td>198</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Number with an unused Flip Flop:</td>
<td>145</td>
<td>out of</td>
<td>198</td>
</tr>
<tr>
<td>Number with an unused LUT:</td>
<td>35</td>
<td>out of</td>
<td>198</td>
</tr>
<tr>
<td>Number of fully used LUT-FF pairs:</td>
<td>18</td>
<td>out of</td>
<td>198</td>
</tr>
<tr>
<td>Number of unique control sets:</td>
<td>7</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Synthesis Report Example – Resource Utilization (2)

IO Utilization:

Number of IOs: 43

Number of bonded IOBs: 43 out of 102 42%

Specific Feature Utilization:

Number of BUFG/BUFGCTRLs: 1 out of 16 6%

Number of DSP48A1s: 5 out of 8 62%
Synthesis Report Example – Timing

Timing Summary:

---------------
Speed Grade: -3

Minimum period: 6.031ns (Maximum Frequency: 165.817MHz)
Map Report Example – Resource Utilization (1)

Design Summary

Slice Logic Utilization:

<table>
<thead>
<tr>
<th>Description</th>
<th>Utilization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Slice Registers:</td>
<td>54 out of 4,800 1%</td>
</tr>
<tr>
<td>Number used as Flip Flops:</td>
<td>53</td>
</tr>
<tr>
<td>Number used as Latches:</td>
<td>0</td>
</tr>
<tr>
<td>Number used as Latch-thrus:</td>
<td>0</td>
</tr>
<tr>
<td>Number used as AND/OR logics:</td>
<td>1</td>
</tr>
<tr>
<td>Number of Slice LUTs:</td>
<td>149 out of 2,400 6%</td>
</tr>
<tr>
<td>Number used as logic:</td>
<td>148 out of 2,400 6%</td>
</tr>
<tr>
<td>Number using O6 output only:</td>
<td>133</td>
</tr>
<tr>
<td>Number using O5 output only:</td>
<td>0</td>
</tr>
<tr>
<td>Number using O5 and O6:</td>
<td>15</td>
</tr>
<tr>
<td>Number used as ROM:</td>
<td>0</td>
</tr>
<tr>
<td>Number used as Memory:</td>
<td>0 out of 1,200 0%</td>
</tr>
<tr>
<td>Number used exclusively as route-thrus:</td>
<td>1</td>
</tr>
</tbody>
</table>
# Map Report Example – Resource Utilization (2)

## Slice Logic Distribution:

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
<th>Total</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of occupied Slices</td>
<td>58 out of</td>
<td>600</td>
<td>9%</td>
</tr>
<tr>
<td>Number of MUXCYs used</td>
<td>32 out of</td>
<td>1,200</td>
<td>2%</td>
</tr>
<tr>
<td>Number of LUT Flip Flop pairs used</td>
<td>162</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Number with an unused Flip Flop</td>
<td>109 out of</td>
<td>162</td>
<td>67%</td>
</tr>
<tr>
<td>Number with an unused LUT</td>
<td>13 out of</td>
<td>162</td>
<td>8%</td>
</tr>
<tr>
<td>Number of fully used LUT-FF pairs</td>
<td>40 out of</td>
<td>162</td>
<td>24%</td>
</tr>
<tr>
<td>Number of unique control sets</td>
<td>7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Number of slice register sites lost to control set restrictions</td>
<td>35 out of</td>
<td>4,800</td>
<td>1%</td>
</tr>
</tbody>
</table>

## IO Utilization:

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
<th>Total</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of bonded IOBs</td>
<td>43 out of</td>
<td>102</td>
<td>42%</td>
</tr>
</tbody>
</table>
Map Report Example – Resource Utilization (3)

Specific Feature Utilization:

Number of RAMB16BWERs: 0 out of 12 0%
Number of RAMB8BWERs: 0 out of 24 0%
……
Number of DSP48A1s: 5 out of 8 62%
……
## Post-PAR Static Timing Report

Clock to Setup on destination clock clk_i

<table>
<thead>
<tr>
<th>Source Clock</th>
<th>Dest: Rise</th>
<th>Dest: Rise</th>
<th>Dest: Fall</th>
<th>Dest: Fall</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk_i</td>
<td>7.530</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## PAR Report

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Check</th>
<th>Worst Case</th>
<th>Best Case</th>
<th>Timing</th>
<th>Score</th>
</tr>
</thead>
<tbody>
<tr>
<td>Autotimespec constraint for clock net clk</td>
<td>SETUP</td>
<td>N/A</td>
<td>7.530ns</td>
<td>N/A</td>
<td>0</td>
</tr>
<tr>
<td>_i_BUFGP</td>
<td>HOLD</td>
<td>0.457ns</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
Timing Report (1)

Timing constraint: Default period analysis for net "clk_i_BUFGP"
3354 paths analyzed, 309 endpoints analyzed, 0 failing endpoints
0 timing errors detected. (0 setup errors, 0 hold errors)
Minimum period is 7.530ns.

--------------------------------------------------------------------------------
Delay (setup path): 7.530ns (data path - clock path skew + uncertainty)
Source: a_register/q_o_4 (FF)
Destination: x_reg_inst/q_o_3 (FF)
Data Path Delay: 7.453ns (Levels of Logic = 2)
Clock Path Skew: -0.042ns (0.513 - 0.555)
Source Clock: clk_i_BUFGP rising
Destination Clock: clk_i_BUFGP rising
Clock Uncertainty: 0.035ns
## Timing Report (2)

Maximum Data Path at Slow Process Corner: `a_register/q_o_4` to `x_reg_inst/q_o_3`

<table>
<thead>
<tr>
<th>Location</th>
<th>Delay type</th>
<th>Delay (ns)</th>
<th>Physical Resource</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLICE_X4Y36.AQ</td>
<td>Tcko</td>
<td>0.447</td>
<td><code>a_register/q_o&lt;4&gt;</code></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><code>a_register/q_o_4</code></td>
</tr>
<tr>
<td>DSP48_X0Y3.B4</td>
<td>net (fanout=21)</td>
<td>1.194</td>
<td><code>a_register/q_o&lt;4&gt;</code></td>
</tr>
<tr>
<td>DSP48_X0Y3.M3</td>
<td>Tdspdo_B_M</td>
<td>3.364</td>
<td><code>Mmult_mult_unsigned</code></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><code>Mmult_mult_unsigned</code></td>
</tr>
<tr>
<td>SLICE_X8Y39.C4</td>
<td>net (fanout=1)</td>
<td>2.050</td>
<td><code>x_reg_inst/q_o&lt;3&gt;</code></td>
</tr>
<tr>
<td>SLICE_X8Y39.CLK</td>
<td>Tas</td>
<td>0.398</td>
<td><code>Mmux_x_57</code></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><code>Mmux_x_4_f7_2</code></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><code>Mmux_x_2_f8_2</code></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><code>x_reg_inst/q_o_3</code></td>
</tr>
</tbody>
</table>

Total: 7.453ns (4.209ns logic, 3.244ns route) (56.5% logic, 43.5% route)
Timing Report (3)

--------------------------------------------------------------------------------
Delay (setup path): 7.484ns (data path - clock path skew + uncertainty)
  Source: a_register/q_o_7_1 (FF)
  Destination: x_reg_inst/q_o_3 (FF)
Data Path Delay: 7.391ns (Levels of Logic = 2)
Clock Path Skew: -0.058ns (0.513 - 0.571)
Source Clock: clk_i_BUFGP rising
Destination Clock: clk_i_BUFGP rising
Clock Uncertainty: 0.035ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
  Total System Jitter (TSJ): 0.070ns
  Total Input Jitter (TIJ): 0.000ns
  Discrete Jitter (DJ): 0.000ns
  Phase Error (PE): 0.000ns
## Timing Report (4)

Maximum Data Path at Slow Process Corner: a_register/q_o_7_1 to x_reg_inst/q_o_3

<table>
<thead>
<tr>
<th>Location</th>
<th>Delay type</th>
<th>Delay(ns)</th>
<th>Physical Resource Logical Resource(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLICE_X2Y33.AQ</td>
<td>Tcko</td>
<td>0.447</td>
<td>a_register/q_o_7_2</td>
</tr>
<tr>
<td>DSP48_X0Y3.B7</td>
<td>net (fanout=13)</td>
<td>1.132</td>
<td>a_register/q_o_7_1</td>
</tr>
<tr>
<td>DSP48_X0Y3.M3</td>
<td>Tdspdo_B_M</td>
<td>3.364</td>
<td>Mmult_mult_unsigned</td>
</tr>
<tr>
<td>SLICE_X8Y39.C4</td>
<td>net (fanout=1)</td>
<td>2.050</td>
<td>mult_unsigned&lt;3&gt;</td>
</tr>
<tr>
<td>SLICE_X8Y39.CLK</td>
<td>Tas</td>
<td>0.398</td>
<td>x_reg_inst/q_o&lt;3&gt;</td>
</tr>
</tbody>
</table>

---

Total 7.391ns (4.209ns logic, 3.182ns route) (56.9% logic, 43.1% route)