ECE 545

Remaining Tasks
Grading Scheme

• Homework - 15%

• Midterm Exam - 20%

• Class Activity - 5% bonus points

• Final Exam - 30%

• Project - 35%
Final exam

✓ 2 hours 45 minutes

✓ in class

✓ design-oriented

✓ practice exams available on the web

Date:

Thursday, December 11, 4:30-7:15pm
ECE 545 Final Exam
Allowed Materials

- Textbooks and printouts of textbook chapters
- VHDL Instructions: Templates & Examples (you are responsible for printing it by yourself)
- One page double-sided cheat-sheet (signed before the exam, and submitted at the end of the exam)
Typical Exam Problems

1. (pseudocode, interface) => block diagram
2. interface (w/ division into Datapath and Controller)
3. (pseudocode, interface, block diagram) => ASM chart
4. actions => control signals
5. timing waveforms based on ASM charts & inputs
6. timing analysis (execution time, latency, throughput, critical path)
7. VHDL code of controllers
8. memories in Xilinx FPGAs
9. combinational and sequential circuit building blocks
Project Deadline (Firm)

Monday, December 15, 11:59 PM