GEORGE MASON UNIVERSITY
ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT
SPRING 2009

ECE 586: DIGITAL INTEGRATED CIRCUIT ANALYSIS AND DESIGN

R 7:20 -10:00 pm Room R -A246

Instructor: Dimitris Ioannou, ST2 Room # 247, tel. 993-1580, dioannou@gmu.edu

Office Hours: R 6:00-7:00 pm; plus other times by appointment

Textbook: "CMOS DIGITAL INTEGRATED CIRCUITS"
Rec.: “Chip Design for Submicron VLSI: CMOS Layout and Simulation”
John P. Uyemura (Thomson, 2006)

COURSE OUTLINE

1. MOSFET operation and SPICE modeling
2. CMOS inverters: static characteristics
3. CMOS inverters: dynamic operation
4. Combinational MOS logic circuits
5. Basics of Layout and Design Rules
6. Sequential CMOS logic circuits
7. Dynamic CMOS logic circuits
8. Semiconductor memories
9. Low Power CMOS
10. BiCMOS logic circuits
11. Chip input and output circuits
12. Chip design methodologies (introduction to ECE 680)

Grading
Homework / projects - 20%
Midterm - 40%
Final - 40%