Final Exam
25 points total

May 16, 2011

Problem 1 (7 points)

1. Draw a detailed block diagram for a 4-bit *unsigned* Radix-2 Sequential Multiplier with Carry Save Adder based on the Shift/Add Algorithm, Right-Shift version, capable of computing $p = a \cdot x + y$, where a, x, and y are all 4-bit unsigned numbers.
2. Mark the critical path (or paths) in your circuit.
3. Determine values of all control signal during all clock cycles necessary for initializing the circuit and computing $p = a \cdot x + y$.
4. Write a detailed formula for the minimum latency of this multiplier as a function of delays of basic logic components.

Assume that:

a. you can use only D-flip flops, Full Adders, Half-Adders, Modified Half-Adders, 2-to-1 multiplexers, and basic logic gates (NOT, AND, OR, and XOR)

b. the design should be optimized for the minimum product of latency times area

c. in your diagram you can use connections by name, i.e., two nodes with the same name are connected without drawing a line between them

d. you do not need to design the corresponding control unit, but you should give name to all control signals required by your design

e. all outputs from the controller are registered

f. you should assign names and denote widths for all signals and buses in your design.

Problem 2 (3 points)

Show all operands, intermediate values and the final results (in binary representation) generated during the *non-restoring unsigned* division of an 8-bit dividend, z, by a 4-bit divisor, d, for the case of

$$z = 158 \text{ and } d=10.$$

Problem 3 (5 points)

1. Derive the formulas for the *latencies* (in nanoseconds) and *throughputs* (in operations per seconds) of the following arithmetic circuits *without pipelining*:

   a. 16-bit Brent-Kung Adder
   b. 8x8-bit unsigned array multiplier
   c. 8x8-bit unsigned systolic bit-serial multiplier

2. Which of the listed above circuits can be pipelined?

3. For all circuits that can be pipelined, derive the formulas for *latencies* and *throughputs* of the corresponding circuits after pipelining.

Assume that all circuits are composed of Full Adders, Half-Adders, Modified Half-Adders, 2-to-1 multiplexers, basic logic gates (NOT, AND, OR, and XOR), and D flip-flops. You can use the delays of each of these components, e.g. d_{XOR}, $d_{FAcin->cout}$, d_{FF}, etc., and the setup time of a D flip-flop, t_{setup}, in your formulas.

Problem 4 (6 points)

Design a 4x4 unsigned squarer mod 15, i.e., the circuit that performs operation

$$s=a^2 \bmod 15$$

for a 4-bit input a.

As intermediate steps in your design, please provide:
a) table of partial products,
b) dot diagram, and
c) detailed block diagram.

Assume that you can use the following components in your block diagram: Full Adders, Half-Adders, Modified Half-Adders, 2-to-1 multiplexers, and basic logic gates (NOT, AND, OR, and XOR).

Your optimization target should be the minimum product of latency times area.

Problem 5 (4 points)

Convert the following numbers between representations, using the best known to you algorithms

a. from the 16-bit unsigned binary representation to the 8-digit radix-4 signed Booth representation

   number to be converted: 1101 1011 1110 0110

b. from the 8-bit binary signed digit (BSD) representation to the 8-bit signed binary two's complement representation

   number to be converted: -1 -1 1 1 -1 1 1 -1

Is an overflow possible during any of these conversions? If so, how would you detect it.

Bonus Problem 1 (bonus 2 points)

Redraw your block diagram from Problem 1 under the assumption that all operands, i.e., *a*, *x*, and *y,* are 4-bit signed numbers in the two's complement representation.

Bonus Problem 2 (bonus 2 points)

Explain how would your block diagram from Problem 4 change, if the input *a* was a signed number given in the two's complement representation. Draw any part of the block diagram that would need to be added or modified.