Midterm Exam 1
15 points total

March 25, 2002

Part I
Multiple-Choice Test

1. **(1 point)** Match the following 6-bit representations of -25 with the names of these representations:

A. 100111
B. 111001
C. 110101
D. 100110
E. 000111

a. biased with $B=2^5$
b. one's complement
c. two's complement
d. signed magnitude
e. unknown

2. **(1 points)** Arrange the following signals in the order they are generated within the 64-bit 3-level carry lookahead adder shown in *Parhami*, Fig. 6.5, starting from the signal that is generated first. Assume that the adder is built of AND, OR, and XOR gates, and that delays of all these gates are equal.

A. $p_{[20,23]}$
B. s_3
C. g_{63}
D. c_{32}
E. s_{37}

3. **(1 points)** Arrange the following 16-bit adders in the order of the increasing number of gates. Assume that all adders are built of AND, OR, and XOR gates. Every adder accepts carry-in and produces carry-out.

A. Kogge-Stone parallel prefix network adder
B. Brent-Kung parallel prefix network adder
C. ripple-carry adder
D. 1-level carry-skip adder with 4-bit skip blocks

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4. **(1 point)** Determine the longest path carry propagates through during the addition of the following two 16-bit numbers. Your answer should include the bit position where carry is generated, and the bit position where carry is annihilated.

   0101 0110 1101 1111
   0101 1001 1010 1011

5. **(2 points)** Using dot notation, show the addition of seven 4-bit numbers in the Wallace Carry-Save tree.

Part II
Short Problems
(3 points for each problem)

1. Design a 6-bit adder using a hybrid Brent-Kung/Kogge-Stone parallel prefix network built of AND, OR, and XOR gates with up to four inputs, supplemented with additional gates of the same type. Estimate the delay of this adder expressed in the number of gate levels.

2. Design the maximum-size two-level carry-skip adder with the worst-case delay of 6 time units. Assume that each of the following operations takes one unit of time: generation of g_i and p_i signals, generation of a level-*i* skip signal from level-(*i*-1) skip signals, ripple, skip, and computation of sum bit once the incoming carry is known.

3. Design a minimum-area 6-bit counter that in every clock cycle increments its value by 6, and resets to zero after exceeding 60. Assume that you can use AND, OR, XOR and XNOR gates. Estimate the total number of gates necessary to build the combinational portion of this circuit (i.e., without counting registers). Assume that you have available registers with the synchronous reset signal.