Midterm Exam 1
20 points total

March 28, 2005

Part I
Analytical Problems

1. **(1 point)** Arrange the following numbers in the ascending order:

   A. $(3\ -2\ 1\ -2)_4$
   B. $(179.45)_{-10}$
   C. $(220)_8$
   D. $(321.50)_{1/10}$
   E. $(1\ 1\ 0\ -1\ 1\ -1\ 1)_2$

2. **(1 point)** Arrange the following signals in the order they are generated within the 16-bit Brent-Kung adder, starting from the signal that is generated first. Assume that the adder is built of AND, OR, and XOR gates, and that delays of all these gates are equal.

   A. $p_{[0..5]}$
   B. s_4
   C. $g_{[0..2]}$
   D. c_{13}
   E. s_{12}

3. **(2 points)** Arrange the following 12-bit adders in the order of the increasing number of gates. Assume that all adders are built of AND, OR, and XOR gates. Every adder accepts carry-in and produces carry-out.

   A. 1-level carry-select adder
   B. 2-level carry-select adder
   C. Kogge-Stone parallel prefix network adder
   D. Brent-Kung parallel prefix network adder
   E. Hybrid Brent-Kung/Kogge-Stone adder

4. **(2 points)** Compute the product of the following two elements of the Galois Field $GF(2^8)$: 'A6' and 'B8'. Assume that an irreducible polynomial P(x) is equal to $P(x)=x^8+x^4+x^3+x+1$

5. **(2 points)** Determine all bits of the ANSI/IEEE standard single-precision representation of the following numbers:

   a. 250.53125_{10}
   b. 0 ×infinity

c. $-1.2345_{10} / 0$
d. $-1.011011_2 \times 2^{-140}$

Part II
Design Problems
(4 points for each problem)

1. Design a 12-bit adder using a hybrid Brent-Kung/Kogge-Stone parallel prefix network built of NOR gates with up to four inputs, supplemented with additional gates of the same type. Estimate the delay of this adder expressed in the number of gate levels, and its area expressed in the number of NOR gates.

2. Draw sketch block diagrams and derive detailed formulas for the minimum latency of the 64-bit
   a. Bit-serial adder
   b. Digit-serial adder with the digit size d=8
   c. Incrementer
   d. Decrementer,

   assuming that
   - all circuits are built of NAND gates and D flip-flops only,
   - inputs and outputs of all circuits are stored in registers or shift registers based on D flip-flops,
   - the propagation delay of the D flip-flop and its setup time are both equal to the delay of a NAND gate,
   - the unit of latency is a delay of a single NAND gate.

   Clearly formulate all assumptions used in your derivations.

3. Using dot notation, show the addition of seven 4-bit numbers in the Dadda Carry-Save Adder tree. Draw a detailed schematic of the entire adder corresponding strictly to your dot diagram, using only full adders, half adders, and NAND gates. Estimate the delay and area of your circuit, assuming that the full adders and half adders are built of NAND gates.