Midterm Exam 1
20 points total

March 26, 2007

Part I
Analytical Problems

1. **(2 points)**
   A. Represent the following negative number, -103.6875, using
      a. signed magnitude representation,
      b. biased representation with the bias $B=2^7$,
      c. two's complement representation,
      d. one's complement representation,

      all with 8 bits in the integer part and 4 bits in the fractional part.
   B. Extend the obtained representations to the equivalent representations with 16 bits in the integer part and 8 bits in the fractional part.

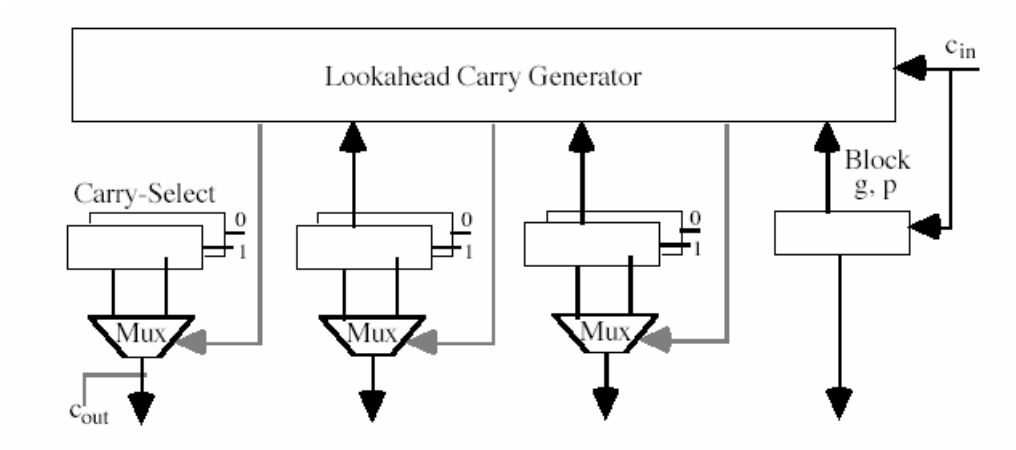
2. **(2 points)** Compute value of the expression $C='2'\cdot A^2$ in the Galois Field $GF(2^4)$ for A='D'. Assume that an irreducible polynomial P(x) is equal to $P(x)=x^4+x^3+1$.

3. **(2 points)** Determine all bits of the ANSI/IEEE standard single-precision representation of the following numbers:

   a. 5/0 + (-5)/0
   b. $-0.0ABCDEF8_{16} \times 16^{-31}$
   c. $-AB.CDEF8_{16} \times 16^{+31}$
   d. $AB.CDEF8_{16} \times 16^{-33}$

   Hint: Use the default IEEE rounding scheme whenever appropriate.

4. **(2 points)** Arrange the listed below signals in the order they are generated within the 16-bit Hybrid Carry-Lookahead/Carry-Select Adder shown in the figure below. For each signal calculate the time when this signal becomes stable for arbitrary values of inputs, assuming that all inputs change at the time 0.
   Assume that
   - Carry-select portion of the adder is based on ripple-carry adders.
   - Carry-lookahead portion of the adder is based on the circuits responsible for generating block generate/propagate signals and a Lookahead Carry Generator.
   - The adder is built out of AND, OR, and XOR gates with up to 4 inputs, and the delays of all these gates are equal.



A. $p_{[8, 11]}$
B. c_{out}
C. c_{12}
D. c_5
E. s_8

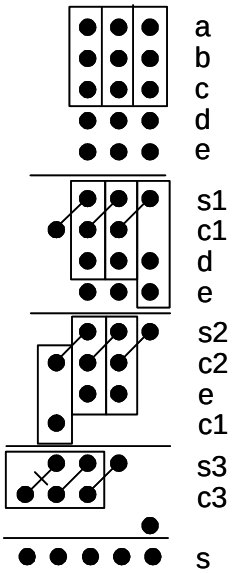
Part II
Design Problems
(4 points for each problem)

1. Derive a general formula for the ratio of the entire areas of a k-bit Kogge-Stone Adder and a k-bit Brent-Kung Adder. Compute the value of this ratio for k=16, 64, and 256.
   Assume that:
   - inputs to the adders are x_i, y_i, cin=c_0, and outputs are s_i, cout=c_k
   - k is of the form $k=2^m$
   - adder is composed of inverters and AND, OR, and XOR gates with up to 4 inputs
   - areas of individual gates (including an inverter) are proportional to the number of inputs
   - unit of area is an area of a 2-input gate.

2. Design a k-bit bit-serial incrementer optimized for minimum area and composed of 2-input NOR gates only.
   Assume that
   - your circuit does not include any surrounding shift registers or registers
   - control signals, such as START, are provided externally
   - all inputs, including control inputs, are registered (outside of your circuit)
   - D flip-flop is composed of 6 2-input NOR gates, has a clock-to-output delay of 2 NOR gate delays, and the setup time of 1 NOR gate delay
   - unit of delay is a delay of a 2-input NOR gate
   - unit of area is an area of a 2-input NOR gate

   Perform the following tasks:
   a. Draw a block diagram of this circuit using medium level components, such as multiplexers, half-adders, modified half-adders, full-adders, flip-flops, etc.
   b. Draw a detailed schematic of all combinational components of your circuit (no schematic required for a flip-flop).
   c. Determine areas and delays of all combinational components of your circuit.
   d. Determine general formulae for the Clock Period, Latency, and Area of your incrementer as a function of k.

3. Translate the following dot diagram into the corresponding digital circuit.



Perform the following tasks:

a. Draw a block diagram of this circuit using medium level components, such as full-adders and half-adders.
b. Clearly mark names and indices of all signals in your schematic, using notation such as a_0, b_1, $s1_0$, $c2_3$, etc.
c. Mark the critical path of this circuit in your schematic
d. Determine the length of this critical path.
e. Determine the area of this circuit.

Assume that

- full adder is built of two half-adders and an OR gate
- half adders are built of AND, OR, and XOR gates
- delays of all gates are the same
- areas of individual gates (including an inverter) are proportional to the number of inputs
- unit of area is an area of a 2-input gate.
- unit of delay is a delay of a 2-input gate.