Part I (3 points)

Answer the following questions:

1. Describe shortly and compare the ways of extending operations on unsigned numbers into operations on signed numbers for hardware multiplication and hardware division.
2. Explain the need for and describe the method of normalizing a dividend and a divisor in the Radix-4 SRT division. Describe in detail any necessary precomputations, postcomputations, and changes introduced to the division itself.
3. Explain and describe differences between using Carry Save Adders in radix-2 sequential multipliers vs. radix-2 sequential dividers? For which of these two operations Carry Save Adders give a greater speed-up compared to classical sequential circuits?

Part II (12 points)

Develop and debug <u>synthesizable Register Transfer Level</u> (RTL) VHDL code for **one** of the following two arithmetic units:

A. k-bit <u>unsigned radix-4 sequential multiplier with Booth's recoding</u>

B. <u>unsigned fractional radix-2 divider with partial remainder stored in the carry-save form (see Parhami, Fig. 14.8)</u>. The divider should support a 2k-bit fractional dividend and a k-bit fractional divider.
Your circuit should check for an overflow condition, and have an overflow output.

Please perform the following tasks:

1. Draw a detailed schematic of your circuit for k=4.

2. Draw an ASM chart or state diagram describing the behavior of the control unit of your circuit for k=4.

3. Check the functionality of your VHDL code for k=4 and k=16 using at least three different test vectors in each case.

4. Set the target FPGA device to Spartan 2, XC2S100-5TQ144C. Synthesize your codes for k=4 and k=16 using Synplify Pro, and implement them using Xilinx ISE. Perform the timing simulation of your circuit using the same test vectors you used for the functional simulation. Check thoroughly all implementation reports.

5. For both versions of your circuit (with k=4 and k=16), determine their minimum latency and the number of CLB slices required for their implementation.

Please submit the following deliverables:

1. block diagram of your circuit for k=4
2. ASM chart or state diagram describing the control unit of your circuit for k=4
3. source codes of the
   - main circuit
   - test circuit (if any)
   - testbench
4. waveforms demonstrating the correct <u>timing</u> simulation of your circuits at their maximum clock frequency for three different test vectors
5. short report containing at least the description of the
   - circuit interface
   - test vectors
   - minimum number of CLB slices
   - minimum latency.