Midterm Exam
20 points total

March 27, 2013

Part I
Analytical Problems

1. **(3 points)**
   A. Represent the following negative number, -94.6875, using
      a. signed magnitude representation,
      b. one's complement representation,
      c. two's complement representation,
      d. biased representation with the bias $B=2^{k-1}$-ulp,

   all with k=8 bits in the integer part and l=4 bits in the fractional part.
   B. Extend the obtained representations to the equivalent representations with k'=12 bits in the integer part and l'=8 bits in the fractional part.

2. **(3 points)** Determine all bits of the ANSI/IEEE standard single-precision representation of the following numbers:

   a. $-0.2DDDDDDD_{16} \times 16^{-31}$
   b. $-0.6EEEEEEE_{16} \times 16^{-31}$
   c. smallest positive ordinary number × largest positive ordinary number
   d. (-infinity) × smallest positive denormal

   Hint: Use the default IEEE rounding scheme whenever appropriate.

3. (2 points) Compute value of the expression C='15'·'1A' in the Galois Field $GF(2^5)$. Assume that an irreducible polynomial P(x) is equal to $P(x)=x^5+x^2+1$.

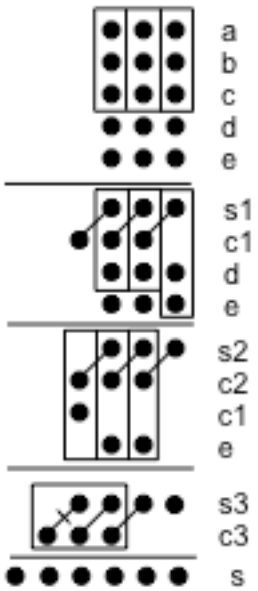
Part II
Design Problems

1. **(4 points)** Draw a full block diagram of the pipelined 8-bit Kogge-Stone Parallel Prefix Network Adder with 7 pipeline stages.
   Derive formulas for the throughput (in additions per unit of a delay), latency, and area of this adder.
   Assume that
   - all inputs are registered (outside of your circuit).
   - your circuit is composed of D flip-flops, AND and OR gates, and inverters only
   - delays of all gates are independent of the number of inputs, and are equal to the delay of an inverter. Thus, you can assume that the delay of each gate and inverter is equal to 1.
   - area of each gate is proportional to the number of inputs. For example, area of a 2-input gate is equal to the area of 2 inverters. Assume that the area of an inverter is equal to 1, area of a 2-input gate is equal to 2, etc.
   - area of a D flip-flop is equal to 12, its clock-to-output delay is equal to 2, and its setup time is equal to 1.

2. **(4 points)** Design a circuit implementing rounding scheme called "Round to nearest, ties to odd (rtno)". Assume that the input is a signed number in the two's complement representation, composed of 8 bits in the integer part and 4 bits in the fractional part. The output is an 8 bit integer and an overflow bit.
   Assume that
   - your circuit is purely combinational, optimized for minimum area, and composed of AND and OR gates, and inverters only
   - you can use AND and OR gates with 2, 3, and 4 inputs only
   - unit of delay is a delay of an inverter
   - unit of area is an area of an inverter
   - all gates have a delay independent of the number of inputs, and area proportional to the number of inputs (e.g., the area of a 2-input gate = 2 × area of an inverter)

   Perform the following tasks:
   a. Draw a block diagram of this circuit using medium level components, such as multiplexers, half-adders, modified half-adders, full-adders, etc.
   b. Draw a detailed schematic of all medium-level components of your circuit
   c. Determine areas and delays of all medium-level components of your circuit.
   d. Determine formulae for the Latency and Area of the entire circuit.

3. **(4 points)** Translate the following dot diagram into the corresponding digital circuit.



Perform the following tasks:

a. Draw a block diagram of this circuit using medium level components, such as full-adders and half-adders.
b. Clearly mark names and indices of all signals in your schematic, using notation such as a_0, b_1, $s1_0$, $c1_3$, etc.
c. Determine the minimum number of 4-input Look-Up Tables (LUTs) necessary to implement this circuit using Xilinx Spartan 3 devices, assuming that
    - Full adders within Carry Save Adders are implemented using LUTs only
    - Full adders within a Carry Propagate Adder and half-adders within both types of adders are implemented using fast carry chain logic (LUT + 2-to-1 MUX + XOR gate)

Bonus (1 point):
Determine the critical path and delay of this circuit assuming that

- the delay of a LUT is 1 ns, the delay of a fast-carry-chain MUX is 0.1 ns from carry in to carry out, and 0.25 ns from the select signal to carry out, and the delay of a fast-carry-chain XOR gate is 0.25 ns
- delays of interconnects should be neglected in your computations.