ECE 645
Spring 2014

Homework 1

due Wednesday, February 5, 4:30PM

Problem 1

Draw a block diagram of a 256-bit 3-stage decrementer (based on Ripple Carry Decrementers) capable of counting down from all ones to zero.

Assume that the sizes of 3 stages are equal to k1, k2, and k3=256-(k1+k2).

Choose optimal values of parameters k1 and k2, minimizing the clock period of this circuit, assuming that:

- $k1 \geq 4$
- the entire circuit is implemented using AND and OR gates (with up to four inputs) and inverters only.
- delays of all gates are independent of the number of inputs, and are equal to the delay of an inverter. Thus, you can assume that the delay of each gate and each inverter is equal to 1.
- Delay of registers is equal to $d_{FF}=2$, and their setup time is equal to $t_{setup}=1$.
- Interconnect delays are assumed to be 0.
- Registers are set to all ones by a global set signal at the beginning of computations.

Clearly specify all timing requirements that must be met by your circuit, and then calculate the optimum values of k1, k2, and k3, minimizing the clock period of this circuit.

Problem 2

Design and analyze a k-bit digit-serial adder (DSA) with the digit size d (a digit serial adder is an adder that in each clock cycle processes d-bits of the operands X and Y, and generates the corresponding d bits of the sum S).

Then, compare this adder with the Ripple Carry Adder (RCA) and the Bit Serial Adder (BSA) in terms of the latency, area, and the latency·area product.

Use the following assumptions:

1. Each adder is
   - an unsigned adder with carry in and carry out using a respective interface shown in slides for Lecture 1: Basic Adders,
   - optimized for minimum latency
   - composed of AND and OR gates (with up to four inputs) and inverters only.

2. Delays of all gates are independent of the number of inputs, and are equal to the delay of an inverter. Thus, you can assume that the delay of each gate and inverter is equal to 1.
3. Area of each gate is proportional to the number of inputs. For example, area of a 2-input gate is equal to the area of 2 inverters. Assume that the area of an inverter is equal to 1, area of a 2-input gate is equal to 2, etc.
4. Area of a D flip-flop is equal to 12, its clock-to-output delay is equal to 2, and its setup time is equal to 1.
5. Do not include the areas of the surrounding input and output registers in your computations.
6. All external control signals are registered.

For each adder:

a. Draw a schematic of this adder composed of medium level components (such as full adders, half adders, multiplexers, D flip-flops, etc.), and the detailed schematic of each medium-level combinational component, implemented using aforementioned gates only.

b. Mark the critical path of each adder. Assume that all inputs to the adders, including all control signals are registered.

c. Determine the area and delays of each medium-level component expressed in terms of the delay and area of an inverter.

d. Derive the general formulas for the minimum clock period, latency and area of all adders, in terms of the parameters k and d. For area: Do not include the areas of the surrounding input and output registers in your computations. For clock period and latency: take the register delay and the register setup time into account for all adders.

e. draw the following three graphs:

1. Latency as a function of k
2. Area as a function of k
3. Latency·area product as a function of k.

Each graph should include lines for the following five adders:

i. Bit Serial Adder – BSA
ii. Digit Serial Adder with d=4 – DSA4
iii. Digit Serial Adder with d=8 – DSA8
iv. Digit Serial Adder with d=16 – DSA16
v. Ripple Carry Adder – RCA.

Assume that k changes as follows:

$k=2^i$, for i=5 to 9.

Bonus Problem 1 (requires knowledge of VHDL or Verilog and FPGA tools, can be submitted by Saturday, February 8, 11:59pm)

Model the ripple-carry adder, bit-serial adder, and digit-serial adder in VHDL or Verilog. Use generics (in VHDL) or parameters (in Verilog) for k and d. Use "+" for the ripple-carry adder and the ripple-carry-adder part of the digit-serial adder.

Surround each adder by registers or shift registers placed at each input and output.

Hint: The choice between a register and a shift register will depend on the type of an adder, and the role of its port.

Synthesize and implement your circuits for the following values of generics:

a. RCA, BSA: k = 32, 64, 128
b. DSA: d=8, k = 32, 64, 128.

Target Xilinx Spartan 6 FPGAs. Use the smallest device of the Spartan 6 family capable of holding any implemented adder for k=128 (in terms of both the resource utilization and the number of inputs and outputs).

Determine

- Minimum clock period
- Latency, and
- Area in LUTs (look-up tables)

after placing and routing for each of the evaluated adders.

Calculate all latencies as a function of the minimum clock period, and the parameters k and d.

Draw the following three graphs:

a. Latency as a function of k
b. Area as a function of k
c. Latency·area product as a function of k.

Each graph should include lines for the following three adders:

i. Bit Serial Adder – BSA.
ii. Digit Serial Adder with d=8 – DSA8
iii. Ripple Carry Adder – RCA.