**List and Format of Project Deliverables**
**ECE 645**
**Spring 2014**

# Hardware Projects
# (with possible software and analytical components)

**Top-level folder:**

<First_Name> .zip

**Second level:**

1_block_diagrams
2_interface
3_ASM_charts
4_source_codes
5_verification
6_ATHENa [BONUS]
7_bug_reports [BONUS]

**The recommended content of these folders is described below:**

**1_block_diagrams**

*Comments:*

A. Please name and label all data buses and control signals in your circuit (at a minimum all inputs and outputs and all control and status signals that appear at the interface between the Controller and Datapath). In order to support debugging of your code, I would also suggest naming all intermediate buses and nodes of the Datapath that appear as signals in your VHDL code.

B. All diagrams must be submitted in PDF.
You can use diagrams copied from the papers themselves, extended with your own labels and drawings, if needed. Please clearly mark all changes you have made to these original diagrams.
You can draw your own diagrams in a graphical editor of your choice (e.g., Xfig, MS Visio, Dia). You can also submit scanned versions of handwritten block diagrams.

C. In the file: hierarchy.txt, please include the list of all block diagram files, starting from the block diagram of your top level unit, down to the block diagrams of your lowest-level components.

D. BONUS: The complete editable versions of block diagrams prepared using a graphical editor will be awarded with bonus points.

**2_interface**

**A_top_level**
**B_division**

**A_top_level**

This is a top-level interface of your circuit. Draw a diagram of your interface, and describe the meanings of all inputs and outputs.

*Comments:*

A. You are free to choose an interface that is most suitable for your Architecture.

B. Your circuit must not exceed the number of pins available in the FPGA device you use for the implementation.

C. Each bus should be able to transfer just one word of input/output per clock cycle.

D. You have a freedom to choose the number, names, and meanings of all control signals.

E. Your modules can work as active or passive components (i.e., read data from passive FIFOs, or be written to by surrounding logic units).

**B_division**

Interface with the division into the Datapath and Controller.

**3_ASM_charts**

*Comments:*

A. If more than one FSM is used, please include a block diagram illustrating communication among all FSMs.

B. As a minimum, please include scans of your handwritten ASM charts and the controller block diagram in the PDF format.

C. BONUS: The complete editable versions of ASM charts prepared using a graphical editor will be awarded with bonus points.

**4_source_codes**

*Comments:*

A. Please include all synthesizable VHDL codes of the Datapath, Controller, and Top-Level Circuit.

B. Please include also a file
source_list.txt
listing all files in the order they should be synthesized (bottom-up).

**5_verification**

In this folder include the following subfolders:

**testbenches**

A. All testbenches used to verify your circuit operation at various levels of hierarchy.

**test_vectors**

B. All test vector files you have used in your verification and debugging.

**programs**

C. All programs (in C, Matlab, or other language) you have used to generate these test vectors (with headers containing full author names and affiliations).

5_ **benchmarking [BONUS]**

Divide this folder into subdirectories corresponding to each individual family, e.g., Virtex-6, Spartan-6, etc.
*Please note that the exact choice of families is specific to your project.*

For each run of ATHENa please include only:
- report_option.txt
- report_execution_time.txt
- report_timing.txt
- report_resource_utilization.txt
- report_summary.txt
- athena_log.txt, and
- the config subfolder.

**6_bug_reports [BONUS]**

In this folder, please include the following subfolders

**1_articles**
**2_ATHENa**
**3_Other**

Each bug report should be placed in a separate subfolder of these directories, and named:

bug_<n>_mm_dd, where
mm_dd represents the month and day when a given problem was discovered,
and <n> is a unique bug number.

For each bug you report, please include short description.

In
**1_articles**
please describe all mistakes you have found in journal/conference articles describing your architecture.

These mistakes can include mistakes in the pseudocode, block diagrams, figures, tables, explanations, etc.

In
**2_ATHENa**
please include all information necessary to recreate the same problem (in particular, the version of ATHENa used, design_config.txt, source files, versions of Xilinx and Altera tools used, simulator used, etc.).

***Please compress all the aforementioned folders into a single .zip file, and submit it using Blackboard***

# Analytical Projects

## 1. Excel files

Excel files containing the results of your comparison (if any).

## 2. Literature

The most important publications used in your analysis (in the form of PDF files).

## 3. Bug reports [BONUS]

Please shortly summarize all mistakes and inconsistencies found in the publications analyzed as a part of this project.