

Recommended Outline of Your Report
ECE 645
Spring 2014

The suggested format of your report is the IEEE journal paper template available at http://www.ieee.org/publications_standards/publications/authors/author_templates.html under Template and Instructions on How to Create Your Paper

Hardware Projects
(with possible software and analytical components)

1. Introduction

What is a primary application of your design?

Why is this application important?

What is a practical value of the obtained results?

2. Previous Work

Who developed an algorithm/architecture you are implementing? When? Where was this work published?

Was this algorithm/architecture implemented before in FPGAs? If so, reference papers with the best results.

What is different about your design or implementation?

3. Background

Provide any background (math, computer arithmetic, cryptography, coding theory, etc.) going beyond the material covered in ECE 645, which is necessary to understand the implemented algorithm/architecture.

4. Algorithm and its parameters

Describe an algorithm you are implementing.

You can use

- Graphics
- Mathematical equations
- Flowcharts
- Pseudocode, etc.,

depending on your algorithm, and the ease of its graphical representation.

Please list major parameters of this algorithm, and specify clearly all parameter values supported by your implementation.

5. Design

5.1 Top-Level Interface

Provide a diagram of the top-level interface, with names, widths, and directions of all ports clearly shown.

5.2 Block diagram

You can simplify your block diagram for the purpose of the report, and divide it into multiple figures.

Discuss any elements of your diagram(s) that may not be immediately clear from looking at the figures themselves.

5.3 Interface with the Division into the Datapath and Controller

Please clearly show all signals exchanged between the Datapath and Controller.

Divide the ports of the top-level unit into those belonging to the Datapath, Controller, or both.

Please clearly show the names, widths, and directions of all signals.

5.4 ASM Chart

Please provide only the first-level ASM chart, with Actions (such as, $C=A+B$), rather than values of control signals written inside of State Boxes and Conditional Output Boxes.

You can simplify your ASM chart for the purpose of the report, and divide it into multiple figures.

5.5 Source Code Chart

Provide a graphical chart of your source codes including the names of your VHDL files and mutual dependencies among them. The top-level unit should be shown at the top, and the basic entities that do not use component instantiations at the bottom.

6. Verification

6.1 Test vectors

Please discuss programs (or other methods) that you used to generate test vectors.

What is a format of test vectors that you used?

6.2 Testbenches

Please describe (in general terms) the functionality of your testbenches.

On the Source Code Chart please mark which entities were verified using separate testbenches.

Differentiate between simple testbenches (generating only input stimuli) and advanced testbenches (comparing actual outputs with expected outputs).

6.3 Status of your code

On the Source Code Chart, please mark using a color code, which source codes have been

- A. Fully verified using functional simulation
- B. Written, but not fully debugged
- C. Not completed at the time of presentation

7. Results

7.1 Timing Analysis

Based on the block diagram of your code, please provide the formulas for:

- A. Latency = execution time for a single input, expressed in clock cycles.
- B. Time between two consecutive operations (in clock cycles). This time should describe how many clock cycles after the start of a given operation for one set of operands you can start the same operation with the second set of operands.
- C. Throughput (in operations per second or input/output bits per second).

Please clearly indicate whether you were able to verify any of these formulas using functional simulation.

7.3 Basic results

For the highest level unit, which you were able to verify for correct functionality, please provide:

- A. resource utilization after placing and routing
- B. numerical values of the following timing parameters, based on the minimum clock period after placing and routing
 - a. Maximum Clock Frequency (in MHz)
 - b. Minimum Latency (in ns)
 - c. Maximum Throughput
 - d. Maximum Throughput/Area Ratio
- C. Excel graphs and charts summarizing all results obtained for all implemented architectures and operand sizes.

7.4 Optimized results [BONUS]

Please present all results obtained using ATHENa.

Your goal should be to implement and optimize your design using at least:

- A. One FPGA family used in the best paper that implemented the same or similar architecture in the past
- B. One modern FPGA family, such as Virtex 6 or Spartan 6.

Please clearly indicate whether you were able to improve any results using ATHENa, or you just used ATHENa in the single_run mode in order to simplify the generation and extraction of results.

8. Analysis of Results

8.1 Comparison with results of other groups

Compare your results with the best results reported earlier in the literature.

Please note that your comparison is valid only if you

- a. use the same or equivalent algorithm
- b. use the same parameter values (e.g., operand sizes)
- c. use the same FPGA family (or better yet the same FPGA device)
- d. use the same or similar interface.

However, if any of these conditions does not hold, you can still make the comparison, just clearly indicate the differences between the compared implementations.

8.2 Analysis of results

Clearly summarize your observations regarding the obtained results.

9. Lessons learned

Please discuss any difficulties you encountered, and any lessons you learned by working on this project.

In particular, please describe any difficulties with:

- a. understanding project resources, including earlier publications
- b. generating test vectors
- c. debugging your circuit
- d. using FPGA tools
- e. using ATHENa (optional)
- f. time management, etc.

10. Conclusions and Future Work

Shortly summarize what you have managed to accomplish as a part of this project.

Discuss any possible extensions to this project.

References

The detailed list of references, following the format described in the IEEE template.

Analytical Projects

1. Introduction

What is a primary subject of your analysis?

Why is this subject important?

Why is it interesting for you?

What could be a practical value of the obtained results?

2. Background

Provide any background (math, computer arithmetic, digital signal processing, cryptography, coding theory, FPGA design, etc.) going beyond the material covered in ECE 645, which is necessary to understand the subject of your analysis.

3. Previous Work

Was this analytical topic investigated in any earlier publications?

If so, reference the most relevant publications (Authors, Title, Book/Journal/Conference/On-line article, Year).

What is different/special/better about your analysis compared to the analyses published to date?

4. Alternative solutions

Introduce and discuss all alternative solutions (algorithms, hardware architectures, implementations, embedded resources, etc.) you are comparing against each other.

Shortly summarize each solution.

5. Criteria

Discuss all criteria you are using to identify the best solution (e.g., throughput, latency, throughput/area, latency*area, area, power, energy, flexibility, scalability, testability, fault-tolerance, ease of implementation, etc.)

6. Assumptions

List any assumptions that you have used in your analysis.

7. Results

Describe the results of your analysis in the form of a comprehensive table(s), graphs, etc.

In particular, your table may have a form of a matrix with Criteria listed in rows, and Solutions listed in columns (or vice versa).

Explain and discuss the contents of your table.

8. Conclusions

Discuss major conclusions from your analysis.

What is a practical value of the obtained results?

9. Future Work

Discuss any possible extensions to this project.

References

The detailed list of references, following the format described in the IEEE template.