GEORGE MASON UNIVERSITY
ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT

Fall 2008       ECE 680: Physical VLSI Design

Time and location: Thursday 7:20 pm – 10:00 pm, Krug Hall 209
Instructor: Qiliang Li, S&T-II, Room 249, Tel 703-993-1596, Fax 703-993-1601 qli6@gmu.edu
Office Hours: Thursday 3:00 – 5:00 pm; other times by appointment.

COURSE OBJECTIVES
This course is to provide the fundamental knowledge on CMOS digital circuit design. From this
course, the students will learn to analyze, design, layout, simulate and optimize transistor-level
digital circuits and systems. The students will use state-of-the-art computer-aided design (CAD)
tools to layout, simulate and verify the circuits.


REFERENCE LIST

COURSE OUTLINE
1. Overview of CMOS VLSI (1/2 week)
2. Manufacturing Process of CMOS Integrated Circuit (1/2 week)
3. CMOS Inverter, Combinational CMOS Logic and Layout (1.5 weeks)
4. Designing Sequential Logic Circuits (2 weeks)
5. Implementation strategies for Digital Integrated Circuits (2 weeks)
6. Coping with Interconnect (2 weeks)
7. Timing Issues of Digital IC (2 weeks)
8. Designing Arithmetic Building Blocks (1 week)
9. Designing Memory and Array structures (1 week)

GRADING
Homework/project - 40%
Midterm Exam - 30%
Final Exam - 30%
The dates of the Midterm exam will be announced in class at least two weeks before the exam, and
will depend on the course progress.