Fall 2009 ECE 680: Physical VLSI Design

Time and location: Wednesday 4:30 pm – 7:10 pm, Thompson Hall 117
Instructor: Qiliang Li
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   Office Hours: Wednesday 2:00 pm – 4:00 pm; other times by appointment.

COURSE OBJECTIVES
This course is to provide the fundamental knowledge on CMOS digital circuit design. From this course, the students will learn to analyze, design, layout, simulate and optimize transistor-level digital circuits and systems. The students will use state-of-the-art computer-aided design (CAD) tools to layout, simulate and verify the circuits.

PREREQUISITES:
- Knowledge of MOSFET and CMOS inverter is required.


REFERENCE LIST

COURSE OUTLINE
1. Overview of CMOS VLSI (1/2 week)
2. Manufacturing Process of CMOS Integrated Circuit (1/2 week)
3. CMOS Inverter, Combinational CMOS Logic and Layout (1.5 weeks)
4. Designing Sequential Logic Circuits (2 weeks)
5. Implementation strategies for Digital Integrated Circuits (2 weeks)
6. Coping with Interconnect (2 weeks)
7. Timing Issues of Digital IC (2 weeks)
8. Designing Arithmetic Building Blocks (1 week)
9. Designing Memory and Array structures (1 week)

GRADING
Homework/project - 40%
Midterm Exam - 30%
Final Exam - 30%
The dates of the Midterm exam will be announced in class at least two weeks before the exam, and will depend on the course progress.