ECE 699: Lecture 2

ZYNQ Design Flow
Required Reading

The ZYNQ Book

• Chapter 3: Designing with Zynq
  (“How do I work with it?”)

Xcell Journal

• Xilinx Unveils Vivado Design Suite for the Next Decade of ‘All Programmable’ Devices,
  by Mike Santarini, issue 79, Q2, 2012
Vivado Design Suite

• 4 years of development and 1 year of beta testing
• first version released in Summer 2012
• scalable data model, supporting designs with up to 100 million ASIC gate equivalents (GEs)
• based on industry standards, such as
  • AMBA AXI4 interconnect
  • IP-XACT IP packaging metadata
  • Tool Command Language (Tcl)
  • Synopsys Design Constraints (SDC)
Productivity Gains

• Synthesis tool **3x faster than Xilinx XST**
• Substantial improvement in **runtime** and **maximum design size** compared to Xilinx ISE
• Vivado Simulator **3x faster than ISim**
• Claimed over **4x run-time improvement** over competing tools
• Much **better visibility** into key design metrics, such as **timing, power, resource utilization**, and **routing congestion** much earlier during the design process
• **Estimates** becomes **progressively more accurate**
• Claimed **15x improvement in debugging time**
Design Entry Methods

- VHDL, Verilog
- System Verilog
- C, C++
- System C
- Matlab
- Simulink
Multidimensional Analytical Placer

ISE:

• **One-dimensional, timing**-driven place-and-route algorithms
• Simulated annealing algorithms that determine **randomly** where the tool should place logic cells
• Does adequate job for FPGAs **below 1 million GEs**

Vivado:

• Modern **multidimensional** analytic placement algorithm
• **Deterministically** finds a solution that primarily minimizes: timing, congestion, and wire length
• Better results, **fewer iterations**
• Efficient **up to 100 million GEs**
## Vivado’s Multidimensional Optimization

<table>
<thead>
<tr>
<th></th>
<th>ISE</th>
<th>Vivado</th>
</tr>
</thead>
<tbody>
<tr>
<td>P&amp;R runtime</td>
<td>13 hrs.</td>
<td>5 hrs.</td>
</tr>
<tr>
<td>Memory usage</td>
<td>16 GB</td>
<td>9 GB</td>
</tr>
</tbody>
</table>

Wire length and congestion

![Image showing comparison between ISE and Vivado for wire length and congestion](image)

Source: Xcell, no. 79, 2012
Hierarchical Chip Planning & Advantages of Standards

- ability to partition the design for processing by synthesis, implementation and verification
- divide-and-conquer team approach to big projects
- design preservation feature enabling repeatable timing results
- access to state of the art third-party EDA tools for tasks such as
  - constraint generation
  - formal verification
  - static timing analysis
Power Optimization and Analysis

- capable of analyzing design logic and removing unnecessary switching activity
- advanced clock gating techniques
- up to 30% reduction in dynamic power
- power estimates at every stage of the design flow
Flow Automation, Not Flow Dictation

- GUI-based **push-button** flow
- GUI-based **step-by-step** analysis at each design stage
- Command line
- Batch
IP Packager, Integrator, and Extensible IP Catalog

- any part of the design (including the entire design) can be turned into a **reusable core at any level of the design flow**:
  - RTL
  - netlist
  - placed netlist
  - placed-and-routed netlist
- **IP-XACT descriptions** easy to integrate into future designs
- **IP Packager** specifies the IP data using **XML file**
- **Extensible IP Catalog** allows users to build their own standard repositories from IP they’ve **created, licensed from Xilinx**, or **licensed from third-party vendors**
High-Level Synthesis

• extensive evaluation of commercial tools for Electronic System Level (ESL) design (including study by research firm BDTI)
• 2010 acquisition of AutoESL Design Technologies, Inc. (25 employees) with flagship product AutoPilot
• Autopilot further developed and fully incorporated into Vivado Design Suite as Vivado HLS
• Design and verification orders of magnitude faster than at the RTL level
• Results dependent on the application domain
Vivado HLS

High Level Language
C, C++, System C

Vivado HLS

Hardware Description Language
VHDL or Verilog
**HLS-Based Development and Benchmarking Flow**

- Reference Implementation in C
  - Manual Modifications (pragmas, tweaks)
  - HLS-ready C code
  - High-Level Synthesis
  - HDL Code
  - Physical Implementation
    - FPGA Tools
    - Netlist
  - Post Place & Route Results
  - Test Vectors
  - Functional Verification
  - Timing Verification
Vivado HLS

- **Starts at C**
  - C
  - C++
  - SystemC

- **Produces RTL**
  - Verilog
  - VHDL
  - SystemC

- **Automates Flow**
  - Verification
  - Implementation

Diagram:
- Functional Specification
  - C Design
  - C Testbench
  - Synthesis
  - RTL Design
  - Verification
    - C Wrapper
  - Packaging
    - Vivado IP Packager
  - Architectural Verification
    - IP Integrator
    - System Generator
    - RTL
## Versions of the Vivado Design Suite

<table>
<thead>
<tr>
<th>Design Phase</th>
<th>Feature</th>
<th>WebPACK\textsuperscript{a}</th>
<th>Design Edition</th>
<th>System Edition</th>
</tr>
</thead>
<tbody>
<tr>
<td>IP Integration and Implementation</td>
<td>Integrated Design Environment (IDE)</td>
<td>Included</td>
<td>Included</td>
<td>Included</td>
</tr>
<tr>
<td></td>
<td>Software Development Kit (SDK)</td>
<td>Included</td>
<td>Included</td>
<td>Included</td>
</tr>
<tr>
<td>Verification and Debug</td>
<td>Vivado Simulator</td>
<td>Included</td>
<td>Included</td>
<td>Included</td>
</tr>
<tr>
<td></td>
<td>Vivado Logic Analyser</td>
<td>-</td>
<td>Included</td>
<td>Included</td>
</tr>
<tr>
<td></td>
<td>Vivado Serial I/O Analyser</td>
<td>-</td>
<td>Included</td>
<td>Included</td>
</tr>
<tr>
<td>Design Exploration and IP Generation</td>
<td>Vivado High-Level Synthesis (HLS)</td>
<td>-</td>
<td>-</td>
<td>Included</td>
</tr>
<tr>
<td></td>
<td>System Generator for DSP</td>
<td>-</td>
<td>-</td>
<td>Included</td>
</tr>
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</table>

Source: The Zynq Book
Zynq Development Setup

Windows / Linux computer
4GB+ RAM
Xilinx design tools (3rd party tools)

Source: The Zynq Book
Basic Design Flow for Zynq SoC

Source: The Zynq Book
Example Hardware System with MIO

Source: The Zynq Book
An Example IP Integrator Block Diagram

Source: The Zynq Book
Hardware and Software Layers of a Zynq Design

Source: The Zynq Book
Introducing an IP Block into a Design

Source: The Zynq Book
Parameterization of the Introduced Block
## Vivado vs. ISE (1)

<table>
<thead>
<tr>
<th>ISE</th>
<th>Vivado</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISE Project Navigator</td>
<td>Vivado IDE</td>
<td>These tools are all used for FPGA and Zynq hardware design. Vivado IDE replaces ISE Project Navigator and PlanAhead in the design flow, and has enhanced functionality and library support. PlanAhead and ISE have similar core functionality, but PlanAhead also has pin and device planning and visualisation facilities.</td>
</tr>
<tr>
<td>PlanAhead</td>
<td>Vivado IDE</td>
<td></td>
</tr>
<tr>
<td>Xilinx Synthesis Technology (XST)</td>
<td>Vivado Synthesis</td>
<td>Vivado Synthesis is an enhanced synthesis tool for 7 series and subsequent devices.</td>
</tr>
<tr>
<td>ISim</td>
<td>Vivado Simulator</td>
<td>Vivado Simulator is visually similar to ISim, but it has a new simulation engine with improved performance.</td>
</tr>
</tbody>
</table>

Source: The Zynq Book
# Vivado vs. ISE (2)

<table>
<thead>
<tr>
<th>Xpower Analyzer</th>
<th>Vivado Power Analyzer</th>
<th>For evaluating the power consumption of designs operating on a target device.</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Generator</td>
<td>System Generator</td>
<td>For block-based DSP design. No significant functional changes, but System Generator systems can now be generated to Vivado IP cores.</td>
</tr>
<tr>
<td>AutoESL</td>
<td>Vivado HLS</td>
<td>Tools for developing IP from high-level C, C++ or System-C descriptions. Vivado HLS represents a rebranded and enhanced version of AutoESL.</td>
</tr>
<tr>
<td>Xilinx Platform</td>
<td>IP Integrator</td>
<td>XPS is used to architect embedded hardware systems using lists, options etc. IP Integrator provides an enhanced graphical environment for undertaking the same task.</td>
</tr>
<tr>
<td>Studio (XPS)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Software</td>
<td>Software Development Kit (SDK)</td>
<td>For software systems development. No changes to the purpose or general functionality of this component.</td>
</tr>
<tr>
<td>Development Kit</td>
<td>(SDK)</td>
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<td>ChipScope</td>
<td>Vivado Logic Analyzer</td>
<td>For probing and inspection of real-time signal behaviour on physical devices. The Vivado Logic Analyzer is underpinned by updated hardware cores.</td>
</tr>
<tr>
<td>iMPACT</td>
<td>Vivado Device Programmer</td>
<td>Tools for scanning the hardware chain and configuring the identified devices by downloading programming files.</td>
</tr>
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</table>
Support for Xilinx Families

ISE

90 nm  Spartan-3, Virtex-4
65 nm  Virtex-5
45 nm  Spartan-6
40 nm  Virtex-6

Vivado

28 nm  Artix-7, Kintex-7, Virtex-7, Zynq 7000

Future families