ECE 699 Software/Hardware Codesign
Midterm Exam
Spring 2015

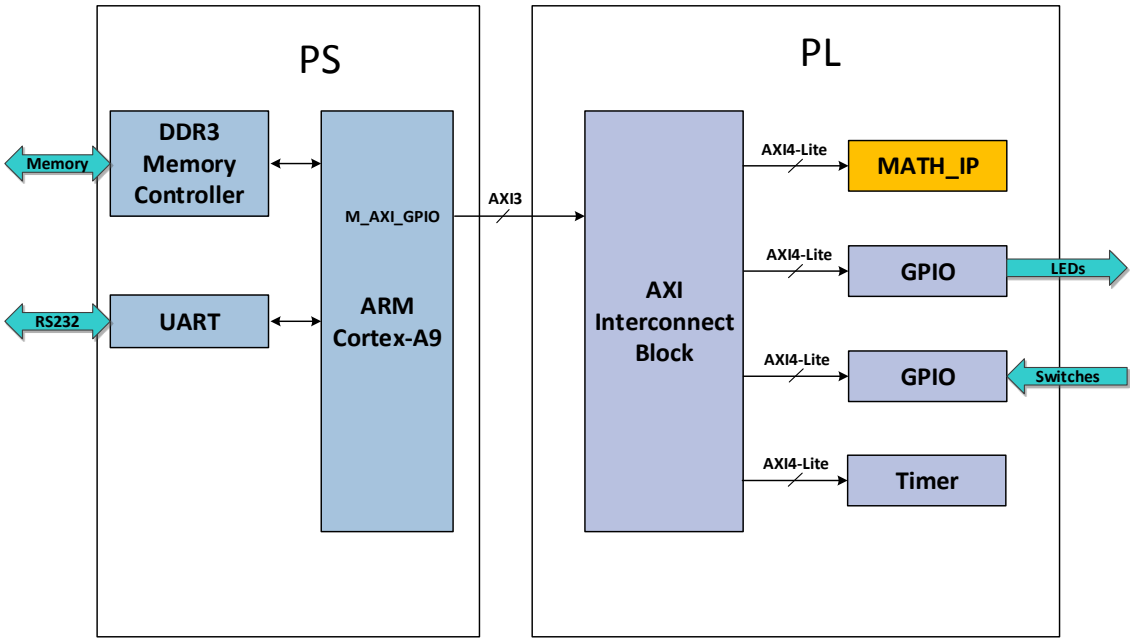
Part 2: Practice

Package the hardware accelerator, called MULT_IP, and build the software/hardware system using already existing IPs mentioned below. Build the complete system and utilize provided C code to view the performance of the system using different parameters, based on the description of the operation given below.

$$P_i = A_i \cdot B_i$$

A_i and B_i are 16-bit operands and result is stored in a 32-bit variable P_i.

1. Simplified Block Diagram



2. Configuration of PS

Configure PS to include the following settings:

1. GP Master AXI interface to talk to hardware IPs.
2. UART interface to view output on the console.
3. DDR3 memory interface to store the arrays.

3. PL Side

Include the following IPs on the PL side:

1. GPIO IP for switch inputs.
2. GPIO IP for LED output.
3. Timer IP to measure the time for HW/ SW codesign approach.
4. Math IP, with AXI-Lite interface, to compute the product of two numbers.
5. AXI-Interconnect IP to connect PS to PL.

Functionality of C code:

Below is the explanation of the functionality of C code.

1. Initialize LEDs and switches.
2. Initialize the timer.
3. Compute array size for A, B and P.
4. Initialize A and B.
5. Compute software results.
6. Compute hardware results.
7. Compare software and hardware results.

Regular Tasks:

1. Build the PL side and export the block design to software.
2. Launch the SDK and include the provided C code.
3. Run the code and view the output on the console for different array sizes. Array sizes for A, B and P are directly controlled from the switch input. Array sizes range between 1 to 2^{sw}(switch value = 0 to 15).

List of deliverable for regular task:

1. Choose the following switch values {1, 2, 4 and 8} and view the output on the console. Copy the results into a word document, called RESULT_DOC, and submit it on Blackboard.
2. 2-minute demo.

Bonus Task:

1. Design the hardware accelerator based on the following description of the operation.

$$P = \sum_{i=0}^{2^{sw}-1} Ai * Bi \bmod 2^{32}$$

   This design should transfer Ai concatenated with Bi to the hardware accelerator using a single 32-bit word. The result is stored in two 32-bit registers.
2. Build the PL side and export the block design to software.
3. Launch the SDK and include the provided C code. Modify the C code to fill the hardware registers appropriately.
4. Run the code and view the output on the console for different array sizes. Array sizes for A, B and P are directly controlled from the switch input. Array sizes range between 1 and 2^{sw} (switch value = 0 to 15).

List of deliverable for regular task:

1. Choose the following switch values {1, 2, 4 and 8}, and view the output on the console. Copy the results into a word document, called RESULT_DOC_BONUS, and submit it on Blackboard.
2. 2-minute demo.