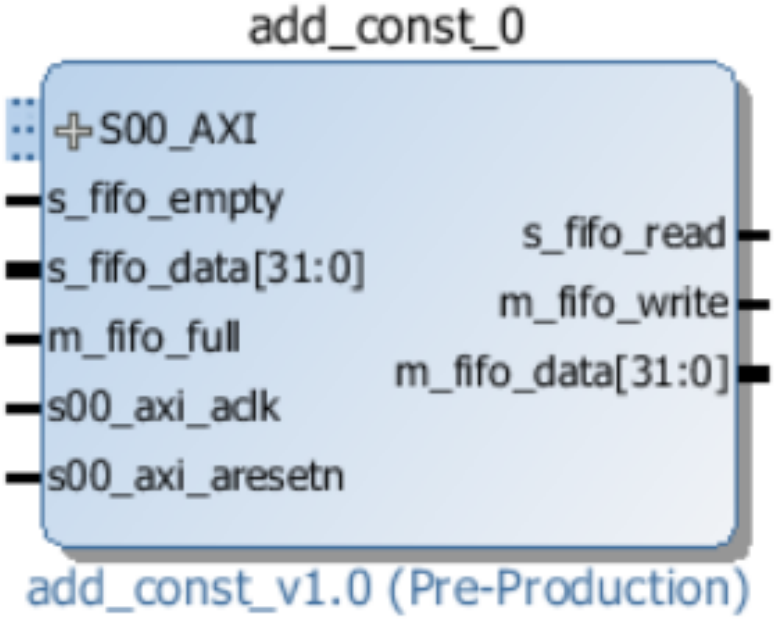
ECE 699: Lecture 7

Custom IP Generation. Efficient Communication Between Custom IPs and PS.

Custom IP Generation

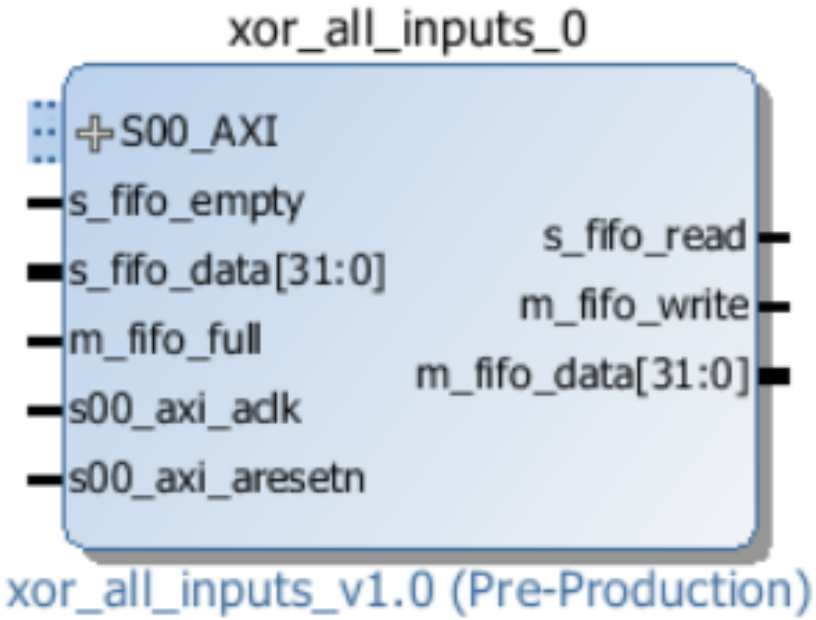
Add Constant IP

- **Input Interface:** AXI Lite, FWFT FIFO
- **Output Interface:** FWFT FIFO
- **Function:** Add a constant value to the input stream of data and put the result into the output.
- The constant value is received using AXI Lite Interface



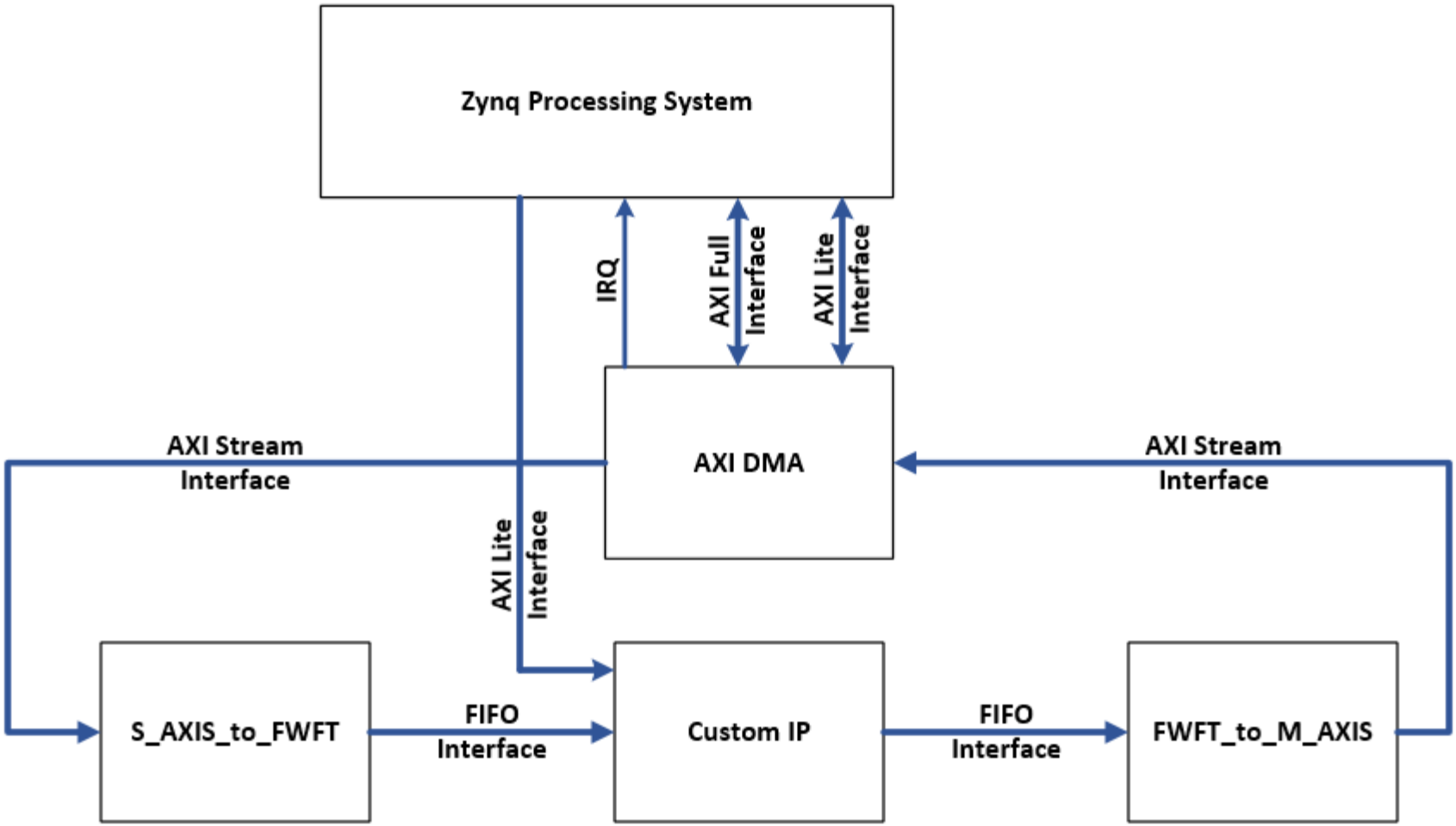
xor all inputs IP

- **Input Interface:** AXI Lite, FWFT FIFO
- **Output Interface:** FWFT FIFO
- **Function:** xor constant number of blocks from input stream and send the result through output stream.
- The constant value is received using AXI Lite Interface

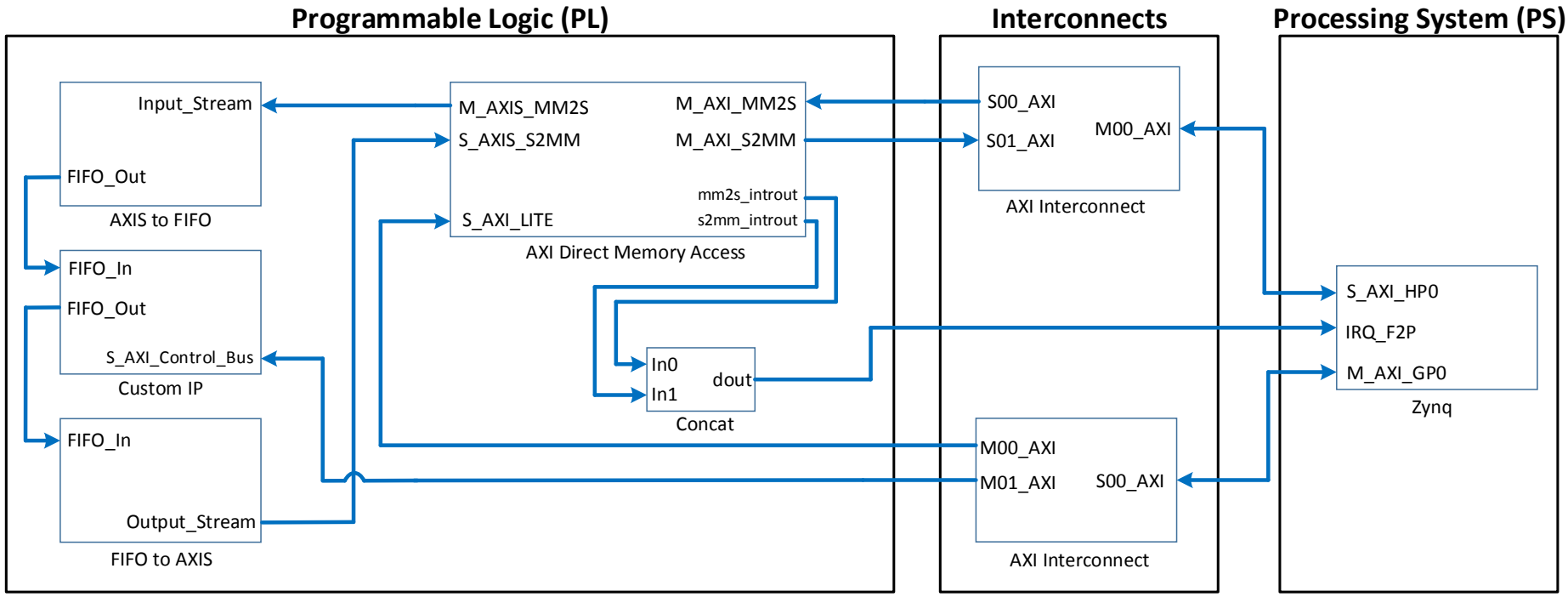


General Approach to Efficient Communication

Simplified Design Flow

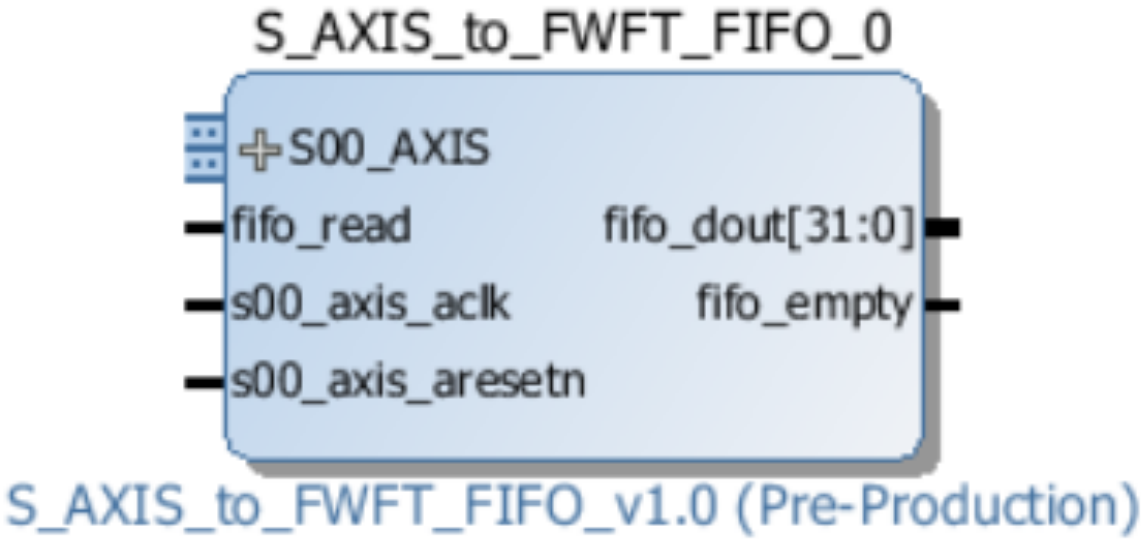


Design Flow


Programmable Logic (PL)
Interconnects
Processing System (PS)
Input_Stream
FIFO_Out
AXIS to FIFO
M_AXIS_MM2S
S_AXIS_S2MM
S_AXI_LITE
M_AXI_MM2S
M_AXI_S2MM
mm2s_introut
s2mm_introut
AXI Direct Memory Access
S00_AXI
S01_AXI
M00_AXI
AXI Interconnect
FIFO_In
FIFO_Out
S_AXI_Control_Bus
Custom IP
In0
In1
dout
Concat
S_AXI_HP0
IRQ_F2P
M_AXI_GP0
Zynq
FIFO_In
Output_Stream
FIFO to AXIS
M00_AXI
M01_AXI
S00_AXI
AXI Interconnect

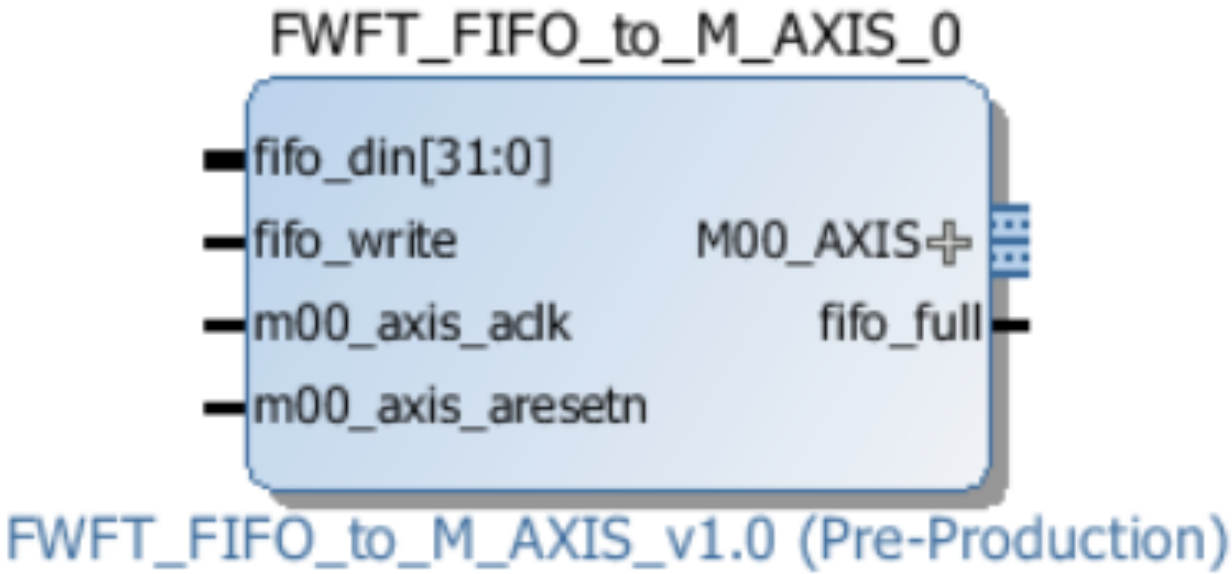
S_AXIS_to_FWFT_FIFO IP

- **Input Interface:** AXI Stream
- **Output Interface:** FWFT FIFO
- **Function:** Contains a FWFT FIFO in which we can write to it using AXI Stream interface and we can read from it using FIFO interface



FWFT_FIFO_to_M_AXIS IP

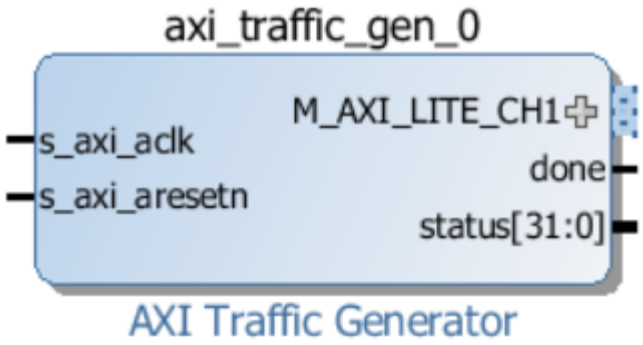
- **Input Interface:** FWFT FIFO
- **Output Interface:** AXI Stream
- **Function:** Contains a FWFT FIFO in which we can write to it using FIFO interface and we can read from it using AXI Stream interface



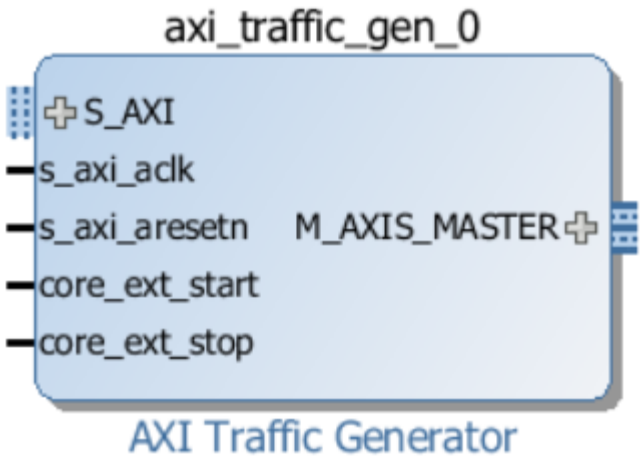
Verification
Using Simulation

AXI Traffic Generator

AXI4-Lite Mode



AXI4-Stream Mode



AXI Traffic Generator

Streaming Config

Streaming Config register allows you to configure the Streaming master interface for programmable delays or random delay in transfer length and TDEST value. This register is only available in the Streaming mode of operation.

Table 2-11: **Streaming Config (0x34)**

Bits	Name	Reset Value	Access Type	Description
31:16	PDLY	~~0x0~~ 0x8	R/W	Programmable delay (in clocks) between two streaming packets.
15:8	TDEST	0x0	R/W	Value to drive on TDEST port.
7:3	Reserved	N/A	N/A	Reserved
2	ETKTS	0x0	R/W	Enable User TSTRB/TKEEP Setting When set, core places your specified STRB/KEEP value on the last beat of the transfer. When this bit is 0, core places internally generated STRB/KEEP value on the last beat of the transfer. You need to set Support Sparse Strobe Keep along with this bit to generate sparse STRB/KEEP values.
1	RANDLY	0x0	R/W	Enable Random Delay When set, generates random delay between streaming transactions. For example, from TLAST to next TVALID.
0	RANLEN	~~0x1~~ 0x0	R/W	Enable Random Length When set, generates streaming transactions with random length. When this bit is 0, core generates the streaming transaction with the length specified in Transfer Length register.

AXI Traffic Generator

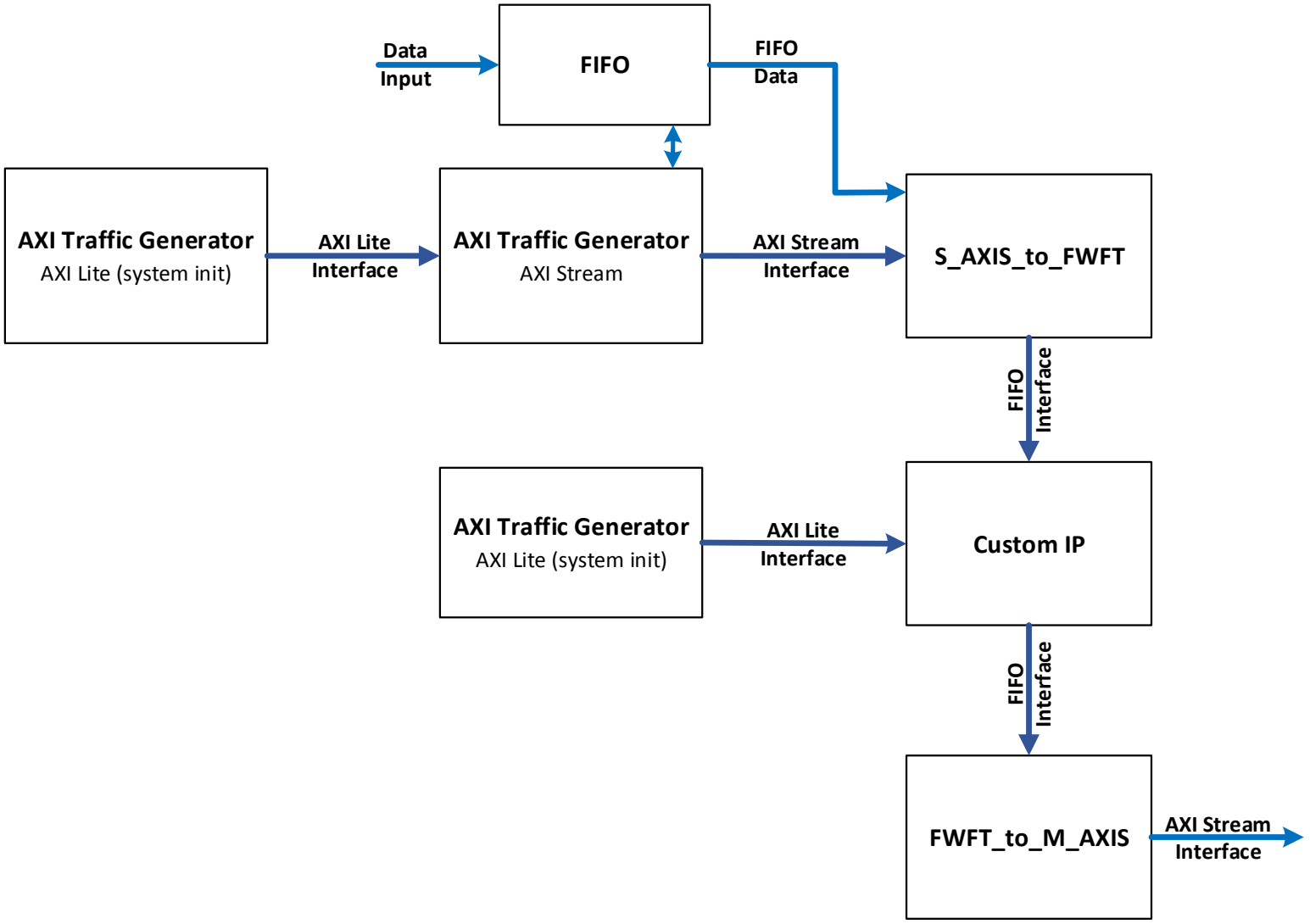
Transfer Length

Transfer Length register allows you to configure the length of packets and transaction count. This register is only available in the Streaming mode of operation.

Table 2-12: **Transfer Length (0x38)**

Bits	Name	Reset Value	Access Type	Description
31:16	TCNT	0x0	R/W	Transaction Count Core generates this many transaction on AXI4-Stream master channel and stops. If set to 0, core infinitely generates transactions.
15:0	TLEN	~~0x0~~ 0x6	R/W	Length of Transaction When Random Length in Streaming Config register is not set, Length programmed in this register is used. Actual number of beats are one more than the register setting. For example, setting to 0 gives 1 beat, setting to 1 gives 2 beats, and further.

Test Circuit Verified Using Simulation



Verification
Using Experimental Testing with Zybo

Simplified Design Flow