

Comparison of the IBM Cell Broadband Engine Architecture to Intel 64/IA-32 Architecture and the Future of Multicore Systems

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I. INTRODUCTION

The Cell Broadband Engine is a new architecture developed by IBM, Sony, and Toshiba. The project was initiated when Sony and IBM executives met in 2000 to discuss the development of a processing architecture that could achieve 1,000 times the performance of the PlayStation 2. The objectives of the new processing architecture included: outstanding performance (especially on multimedia applications), real-time response to user and network, applicability to a wide range of platforms, and support for introduction in 2005.

II. IBM CELL BROADBAND ENGINE

The Cell processor is a heterogeneous architecture that uses a PowerPC element (PPE) as its main general-purpose core. The Cell processor, as built today, contains 8 synergistic processing elements (SPEs) that contain an even more limited RISC instruction set and requires the use of direct memory access (DMA) transfers to move data from main memory into the SPE's large local register file. The PPE, SPE, memory interface controller (MIC), and bus interface controller (BIC) are connected using the element interconnect bus (EIB) which is a ring bus consisting of four 16 byte channels providing a sustained bandwidth of 204.8 GB/s. In addition to the high EIB bandwidth, the memory flow controller connection to XDR memory and the BIC interface to I/O devices connected via RapidIO provide 25.6 GB/s of data bandwidth.

III. INTEL XEON ARCHITECTURE

The Intel quad-core Xeon processors use four symmetric (i.e. identical) cores on a chip as shown in Figure 2.. This is very different from the heterogeneous architecture of the Cell processor. The maximum front-side bus of the current Intel architecture is 1.6 GHz using quad-pumping (transmission on rising and falling edges of two clock signal 90° out of phase) providing a peak bandwidth of 12.8 GB/s. While this number is half that of the Cell processor, the real issue is that data passing across the multiple cores (that do not share the L2 cache) must also use the system bus resulting in a significant performance degradation.

IV. FUTURE OF MULTICORE SYSTEMS

The current focus of processor technology has transitioned from increasing clock frequency to multicore (multiple processing cores on a single die). Part of this transition is due to power and thermal issues of higher clock frequencies in current generation silicon and circuits. One question is whether the future of multicore is the scaling of the current two and four identical core processors. There are indications that the future is not the scaling of current architectures. The IBM Cell Broadband Engine Architecture combines the general-purpose PowerPC core with 8 special-purpose cores. Intel's 80-core tera-scale research processor has multiple general-purpose cores as well as multiple special-purpose cores (dual FPMAC units).

REFERENCES

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