

# **ADC to High Speed FPGA Interface for OC-48**

## **MS CpE Scholarly Paper**

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## **ABSTRACT**

The goal of this project is to sample an analog input and transport the quantized output over SONET interfaces. A highly specialized ADC running at 3.5 Gsps with 8 bits output will be used. This design however will need to accommodate for a 12 bit ADC output in the future. It would therefore be beneficial to know the ADC pinout for the remaining outputs if pinout is going to be preserved moving forward. The outputs of the ADC are source synchronous to the output clock. The outputs will be captured and transported over multiple SONET channels. Since it is important to transport all of the ADC output over the SONET lines without dropping any ADC outputs, we will need to use multiple SONET channels. To optimize the throughput of the SONET payload, the output of the ADC will be placed directly over the SONET payload as concatenated OC48C.

Current requirements call for a single module that takes in analog input and transport the sampled output over multiple SONET optical interfaces. A connector will serve as an interface for the analog input (*Question: What type of connector should this be?*). The analog input signal should be AC coupled before presenting it to the ADC. For the SONET interface, 1550 nm optical interface with FC connector is required.