

A 5-GHz Mesh Interconnect for a Teraflops Processor

Presented By:

Swathy Mudhagouni, Celena Tanguay

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Robinson A 243

Abstract:

A multicore processor in 65-nm technology with 80 single-precision, floating-point cores delivers performance in excess of a teraflops while consuming less than 100 w. A 2d on-die mesh interconnection network operating at 5 GHz provides the high-performance communication fabric to connect the cores. The network delivers a bisection bandwidth of 2.56 terabits per second and a per hop fall-through latency of 1 nanosecond.

The purpose of this paper is to explain Teraflops Processor architecture, On-die interconnect architecture and interconnect design details and how these affect the performance of the microprocessor. The paper will further discuss how the number of cores reflects a trade-off between die size and reaching teraflops performance in a power-efficient manner.