ECE Department

MS EE Scholarly Paper Presentation

3:30 PM, Monday, June 30th, 2008; Room 230A STII

Stress-induced defect generation in HfO_2/SiO_2 Stacks observed by using charge pumping and low frequency noise measurements

By

Shuo Yang

Advisor: Dr. Dimitris Ioannou

Co-Advisor: Dr. Qiliang Li

Abstract

Hafnium-based dielectrics are primary candidates as a replacement of SiO_2 for next generatoin CMOS. However, these materials exhibit a much higher defect density when compared to SiO_2, aggravating some major device reliability issues like bias temperature instability, reduced mobility, and possibly time dependent dielectric breakdown. The knowledge of the trap location and density can improve the understanding of their effects on device reliability.

A novel approach combining the low frequency drain current noise and the frequency-dependent charge pumping techniques has been employed to extract the trap densities in both the interfacial SiO_2 layer and high-k layer in the n-type MOSFETs with HfO_2 /SiO_2 stacks. We monitor the charge pumping and low frequency noise signals, separate the trap in the interfacial SiO_2 and HfO_2, and hence compare the creation of new traps in both layers during the positive and negative stress. It is found that positive bias stress creates more traps in the gate dielectric stack near the gae electrode while negative stress increases the share of traps generated in the proximity to the Si substrate. The results show that under electrical stress new traps are predominantly created close to the anode side and the degree of asymmetry is surprisingly large.