

## A Platform for Building Programmable Multicore Video Processors

Patrick Daderko

ECE641

Thursday November 5, 2009, 6:00pm

Engineering Building, Room 4457

Broadcom's MediaDSP is a scalable multicore platform for creating highly programmable image and video processors. It is a heterogeneous design with task-oriented engines (TOEs), task control units (TCUs), a control engine, and shared memory. The TOEs are the main processing blocks, either with a fixed function or programmable, controlled by its TCU. The control engine is a general purpose RISC controller used to schedule tasks on the TOEs for maximum parallelism.

MediaDSP uses task level parallelism and task based programming to process data. TOEs are assigned a task and do the majority of the data processing in the MediaDSP, and must be programmed in assembly. Control Engines run system and task management code, as well as the ability to do task execution, and are programmed in C. Cache is avoided, and instead memory is transferred through the use of software managed DMA, allowing deterministic timing.

The MediaDSP technology has been used in two commercially available chips. The first was an MPEG audio/video encoder with scaling and noise reduction, using a 7 core design. The second is the BCM35421, a 44 core design, used as a frame rate converter for 120Hz LCD TVs. Among the chip's features are advanced algorithms for motion blur reduction and film judder reduction.