

ECE 611 Final Presentation:

Title: Intel's Larrabee: An x86 Based Many-Core Visual Computing Architecture

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Intel's codename Larrabee is a many-core visual computing architecture from Intel, based on the x86 CPU architecture. It uses multiple in-order x86 CPU cores with wide vector processor units, and several fixed function logic blocks, all connected by a 1024-bit ring bus. It shares many properties with those of general purpose CPUs, as well as those of GPUs. The vector processing unit, where most of the performance comes from, is similar in function to the SSE unit found on most x86 processors, except 4 times larger.

The Larrabee's programming model is similar to that of a multi-core x86 architecture, and therefore, many applications can be recompiled and run on Larrabee without modification. Larrabee Native allows programmers to control low level aspects of the processor using C++ intrinsics or inline Larrabee assembly. Task scheduling is performed in software, as is much of the graphics rendering pipeline, allowing flexibility and specialized performance enhancements. The software renderer is uses a sort-middle algorithm to subdivide tasks into many independent tasks which can be processed in parallel.

Performance analysis of the Larrabee architecture shows significant benefits for highly parallel applications, and those with abnormal data structures. In a ray tracing application, the performance of an 8-core Larrabee at 1GHz was almost twice that of an 8-core Xeon at 2.6GHz. Due to the ability to reconfigure the resource allocation, improved performance and hardware efficiency can be realized across a larger range of applications than those set in hardware.