ECE 681 VLSI Design for ASICs Fall 2013

Class info: Wednesdays, 4:30pm-7:10 pm, Engineering Building 4457
Instructor: Prof. Houman Homayoun
Web: http://cseweb.ucsd.edu/~hhomayoun/
Course website: Materials will post on Blackboard
Email: hhomayou@gmu.edu
Office hours: Monday and Thursday: 3-4 PM
Prerequisite: ECE 545, or permission of instructor.

Course Description
This course introduces VLSI design of application-specific integrated circuits (ASICs) from conceptual design through design release to a foundry using HDL and modern design automation software. Tradeoffs and design perils will be discussed at various phases of this design process. Discussions will include design considerations and tradeoffs made by engineers throughout this process including ASIC performance, power, time to market, design for test, design for manufacturability, etc. Lecture will be accompanied with ample lab time for a hands-on project using the Synopsys tool suite including, synthesis of digital circuits using standard cells, static timing analysis, design for test (test generation/fault simulation), floor planning - placement and routing, clock tree insertion and design rule checking.

Goals in This Class
- Understand challenges with designing very large-scale chips. Understand challenges with deploying new semiconductor technologies.
- Learn industry standard ASIC design flow.
- Learn how to Constrain and Optimize the Design in Synthesis.

Course Content (This is tentative and will change as we progress in the class)
- Aug. 28 Overview of modern VLSI Design Challenges, Flow and Methodology, Overview for Writing Verilog for Synthesis
- Sep.4 Introduction to Synthesis – Libraries, HDL Coding and other Considerations
- Sep. 11 Challenges in Deep Submicron Technologies, Process Variation, Leakage Current, Reliability
- Sep. 18 Memory Circuit and Architecture, SRAM, DRAM, CAM, Non-volatile
- Sep.25 Static Timing analysis, Power Analysis
- Oct. 2 Design For Test, Memory test
- Oct. 9 Mid-term Exam
- Oct. 16 Front-end Design, Synthesis Feedback and Timing Closure
- Oct. 23 Back-end Design, Placement, Routing/Wiring, Post Placement Analysis (timing and power)
- Oct. 16 Design Checking (DRC/LVS/Timing)
- Oct. 23 Paper review on gate and subthreshold leakage in deep submicron technologies
- Oct. 30 Paper review on process variation in deep submicron technologies
- Nov. 6 Paper review on thermal, reliability, and ITD
• Nov. 13 Paper review on NBTI and wear-rout effects
• Nov. 20 Paper review on DRAM, SRAM, STT-RAM circuit technologies
• Nov. 27 Thanksgiving – school break
• Dec. 4 Advanced topic in VLSI: non-volatile logic
• Dec. 11 Final Exam

Literature
• NO TEXTBOOK REQUIRED
• Reading material will be selected from leading conferences, journals, and magazines including TVLSI, GLSVLSI, ISVLSI, DAC, DATE conferences as well as active research projects. All required material will be made available on the course web page.

Grading Policy
• Assignments (8 Labs): (25%)
• Project: (25%)
• Presentation (10%)
  o Student presentation; to be scheduled for each student from the reading list.
• Midterm (15%)
• Final (25%)

Project
TBD.

Reading List
Depending on the number of students in class, each student needs to present 1~2 papers from the reading list. (the reading list includes key papers in Transaction on VLSI, GLVSLI, DAC, DATE Conferences. So you will most likely find slides for these papers online. If not, you can contact the authors, and they will forward you the slides, if they have).

Assignments (Labs)
There will be 8 assignments that are designed to help you learn the standard digital design flow methodology.

Tools:
In this class you will learn how to use these industry level standard design flow tools:
  • Front-end (from synopsys)
  • Back-end (from synopsys)

Helpful text