Course Syllabus

George Mason University
Electrical and Computer Engineering Department

ECE 331: Digital System Design

Instructor: Dr. Craig Lorie
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Teaching Assistants:
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Phone: phone #
Email: sgurung@gmu.edu

Lecture and Recitation Sections

Lecture Tu / Th 12:00 – 1:15 pm Innovation Hall., Room 204
Recitation Sec. 301 M 9:30 – 10:20 am Engineering Bldg., Room 4457
Recitation Sec. 302 M 3:30 – 4:20 pm Science and Tech. II, Room 228
Recitation Sec. 303 F 12:00 – 12:50 pm East Hall, Room 134

Office Hours
Dr. Craig Lorie Monday 2:00 – 3:00 pm Engineering Bldg., Rm. 3221
Wednesday 3:00 – 4:00 pm Engineering Bldg., Rm. 3221
Ahmad Salman Tuesday 5:00 – 9:00 pm Engineering Bldg., Rm. 3203
Smriti Gurung Thursday 9:00 – 1:00 pm Engineering Bldg., Rm. 3203

If you cannot attend the provided office hours, please feel free to contact the TA's or myself via email with questions that you have, or to schedule an alternate meeting time.

Textbook
Authors: Charles H. Roth, Jr. and Larry L. Kinney
Course Objectives
The primary objective of this course is to provide the student with the fundamental concepts and skills necessary to analyze and design combinational and sequential logic circuits. It also introduces the student to the use of a Hardware Description Language (specifically, VHDL) to describe both types of logic circuits. The material covered in the lecture is reinforced through practical experience in the associated lab (ECE 332), including an emphasis on the use of VHDL to synthesize logic circuits.

Topics to be covered in this course:
1. Introduction to VHDL
2. Basic Logic Functions and TTL Gates
3. Boolean Algebra
4. Karnaugh Maps
5. Boolean Expressions – Standard Forms and Minimization
6. Analysis and Design of Combinational Logic Circuits
7. Number Systems
8. Binary Arithmetic and Binary Codes
9. Single-bit and Multi-bit Adder Circuits
10. Multiplexers and Demultiplexers
11. Decoders and Encoders
12. Hazards
13. Latches and Flip-Flops
14. Registers and Counters
15. Analysis and Design of Sequential Logic Circuits
16. An introduction to BJT and MOS Transistors
17. CMOS implementation of Logic Gates
18. Electrical characteristics of Logic Gates
19. Power dissipation and propagation delay

A more detailed schedule of the topics covered in lecture are provided in a separate document.

Recommended background for ECE 331: ECE 280 – Electric Circuit Analysis

The Lab (ECE 332)
The lab must be taken in conjunction with the lecture, or must have been completed previously with a grade of C or better.

Lab Sec. 201 M 10:30 am – 1:20 pm Engineering Bldg., Room 3203
Lab Sec. 202 W 10:30 am – 1:20 pm Engineering Bldg., Room 3203
Lab Sec. 203 R 1:30 pm – 4:20 pm Engineering Bldg., Room 3203
**Homework**
Homework will be assigned on a weekly basis, covering the material discussed in class that week. It is due at the **beginning** of class on the date specified. Homework submitted at the **end** of class will be assessed a **10% penalty**. **No late submissions** will be accepted, as solutions will be posted on the day after it is due. If you have a problem with the submission deadline you must speak to me in advance to make alternate arrangements.

Homework is essential to learning the material. You should make an honest and conscientious effort on all of the homework assignments.

Each homework assignment will consist of **eight** problems. The eight problems will be grades as follows:

1. **Two** problems, selected either by myself or the TA, will be worth 35 points each. Full credit will be given to those solutions that are both correct and complete; partial credit will be given on these problems.
2. The remaining **six** problems will be worth 5 points each. Full credit will be given for a reasonable attempt at a solution; no partial credit will be given on these problems.

You will not be informed as to which two problems will be selected for full grading!

**Exams**
There will be two exams during the course of the semester, as well as a Final exam at the end of the semester. All exams are **closed book**.

There will be **NO** make-up exams. (See Dr. Lorie for an exception).

Exam #1: Thursday, October 7, 2010
Exam #2: Thursday, November 18, 2010
Final Exam: TBD

**Emailing Dr. Lorie:** The subject line of all emails MUST be formatted as follows:

“ECE331 - <last name> <first initial> - <subject of email>”

Failure to do so will delay or prevent a response.

**Course Website:** [http://ece.gmu.edu/~clorie/Fall10/ECE-331/](http://ece.gmu.edu/~clorie/Fall10/ECE-331/)
Grading
Your final grade will be the weighted average of the homework, two semester exams, and the final exam, as calculated from the formula below:

<table>
<thead>
<tr>
<th>Component</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Homework</td>
<td>15%</td>
</tr>
<tr>
<td>Exam #1</td>
<td>25%</td>
</tr>
<tr>
<td>Exam #2</td>
<td>25%</td>
</tr>
<tr>
<td>Final Exam</td>
<td>35%</td>
</tr>
</tbody>
</table>

Letter grades will be assigned according to the following scale:

<table>
<thead>
<tr>
<th>Score Range</th>
<th>Grade</th>
</tr>
</thead>
<tbody>
<tr>
<td>98 – 100</td>
<td>A+</td>
</tr>
<tr>
<td>93 – 97</td>
<td>A</td>
</tr>
<tr>
<td>90 – 92</td>
<td>A-</td>
</tr>
<tr>
<td>87 – 89</td>
<td>B+</td>
</tr>
<tr>
<td>83 – 86</td>
<td>B</td>
</tr>
<tr>
<td>80 – 82</td>
<td>B-</td>
</tr>
<tr>
<td>77 – 79</td>
<td>C+</td>
</tr>
<tr>
<td>73 – 76</td>
<td>C</td>
</tr>
<tr>
<td>70 – 72</td>
<td>C-</td>
</tr>
<tr>
<td>60 – 69</td>
<td>D</td>
</tr>
<tr>
<td>&lt; 60</td>
<td>F</td>
</tr>
</tbody>
</table>

Please note that the final grades will be scaled such that the class average is a 78 (C+) prior to assigning letter grades.

Attendance
Attendance in lecture is highly recommended. The material covered in the lectures will supplement that which is covered in the textbook, provide additional examples to aid in the learning and understanding of the material, and offer you the opportunity to ask questions to clarify the material. Thus, it will benefit you to attend lecture. Should you choose not to attend lecture, you will be responsible for all of the material covered – which you can learn about from one of your classmates. Should class attendance fall below an acceptable level, I reserve the right to conduct “pop quizzes”. You are adults, and as such are expected to make good decisions, ones that will give you the best chance at success.

Attendance in LAB is mandatory!
**Honor Code**
All rules of the GMU Honor Code system will be enforced in both the lecture and the lab. You must review the rules of the GMU Honor Code and be familiar with them.

You are encouraged to discuss homework problems with other students and/or obtain the assistance of the lecture or recitation instructor. Nevertheless, please write down your own solutions which represent your understanding of the material. Duplicating another student's homework solutions, hardware/software designs, diagrams, source code, prelab assignment and exam notes is considered cheating. If you use material from other sources such as but not limited to the web, books, journals, data sheets, etc. you must reference the source.

Honor code violations will be pursued and prosecuted to the fullest extent.

**Classroom Etiquette**
Cellphones are to be turned off during class; minimally they must be silenced. Emergency calls may be taken, but must be taken outside of the classroom.

Texting, using your laptop for something other than lecture-related work, etc. is considered a distraction to me and to the other students trying to learn in the class, and will not be tolerated.

**Students with Disabilities**
If special assistance is required or special accommodations need to be made, please contact me as soon as possible so that the proper arrangements can be made.