Laboratory #Propagation Delay and Power Measurement

ECE 332

1 Introduction

In this lab you are going to observe the propagation delay 2-input AND gate implemented using a TTL IC and a 2-input AND gate implemented in CPLD and compare per gate propagation delay in both technologies. You are also going to measure power consumption of the CPLD when it is implementing the propagation delay circuit at run time.

2 Propagation Delay in TTL technology

Connect the four gates present in 74LS08 Quad2-input AND gate IC as shown in circuit diagram 1. Connect one input of the first AND gate(leftmost) to a square wave or clock source present on the trainer. Tie the second input to 1 i.e. VCC. Connect the output of the final AND gate(right most) to the oscilloscope. Connect clock source to channel 1 and the output from the AND gate to channel 2 of the oscilloscope so that you can visualize the propagation delay easily. Observe the propagation delay as the output of circuit 2 changes from 0 to 1. Note down the propagation delay and per gate propagation delay in the Table 1.

![Circuit Diagram](image)

Figure 1: Circuit Diagram-Implemented on TTL technology

Sketch the clock source and the output wave from as seen in oscilloscope in the graph shown below.
2.1 Propagation Delay in CPLD technology

Implement the circuit diagram shown in 3 in VHDL. Use Structural style of VHDL coding. Make a package which contains VHDL code for AND gate only. Use For-Generate statement in your VHDL code. In the UCF file, connect one input of the first AND gate (leftmost) to clock pin on the CPLD board. Use 10KHz clock frequency. Connect the other input to a switch and keep the switch in HIGH state. Connect the output of the final AND gate (right most) to the LED on the CPLD board.

Figure 3: Circuit Diagram Implemented on CPLD technology

Observe the Post-Fit simulation and note down the delay in change of the output signal with respect to clock input and tabulate the results in Table 1.

2.2 Comparison of Propagation Delay in different technology

<table>
<thead>
<tr>
<th>Technology</th>
<th>Total Propagation Delay</th>
<th>Per Gate Propagation Delay</th>
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</thead>
<tbody>
<tr>
<td>TTL</td>
<td></td>
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<tr>
<td>CPLD</td>
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Table 1: Truth Table for the Circuit

*Note:* Per gate propagation delay = Total Propagation delay / Number of gates
What is your observation from the above table?
2.3 Power measurement

- After downloading the .jed file to the CPLD board using the "Cool Runner Utility Window" proceed with the following steps.

- Uncheck "Vccint" and "Vccio2" and leave "Vccio1" and "Temperature" checked and change C to F.

- From the drop down menu, change the scale of Vccio1 to 50 UA/Div and leave temperature as is.

- Put the 2nd input switch on Off position.

- Make sure that your clock jumper is set to 10 Khz (ask your lab instructor if you need help with this)

- Press Start button.

- Press the "calibrate" button once after making sure that the value in the white box is 75F.

- After the minutes indicator turns from 0 to 1 put the switch back on ON position.

- Wait until the minutes goes to 3 and press the Stop button.

- Read the the Min, AVG and Max current values for VCCio1.

- Calculate Min, AVG and Max power consumption (Note that I/O voltage is 3.3V).