ECE 331 – Digital System Design

Homework #1

due: Wednesday, February 2, 2011

- Write your name at the top of each page of your solutions.
- Clearly indicate the start of the solution for each problem.
- Properly order and staple all pages of your solution.
- Show all of your work!
- A solution that requires physical units is incorrect without them.
- Clearly identify your result (e.g. box or circle the result).
- Always write neatly! If it cannot be read, it will not be graded!

- Always read the associated sections of the textbook before attempting the homework problems!

Additional note for this assignment:

Please draw all circuit and wiring diagrams neatly. If the TA cannot read and/or understand your diagram(s) you will not get credit.

As discussed in class, many of the electrical and timing characteristics associated with standard logic gates are defined for a specific set of conditions. Please include these conditions when reporting the electrical and timing characteristics below.

1. For the 74LS00, specify the following

   (a) The logic operation.
   (b) The truth table.
   (c) The “absolute maximum” supply voltage.
   (d) The voltage range for a logic 0 at the output of the gate.
   (e) The voltage range for a logic 1 at the output of the gate.
   (f) The voltage range for a logic 0 at the input of the gate.
   (g) The voltage range for a logic 1 at the input of the gate.
   (h) The gate delay for the low-to-high transition of the output.
2. For the 74HC02, specify the following

   (a) The logic operation.
   (b) The truth table.
   (c) The “absolute maximum” supply voltage.
   (d) The voltage range for a logic 0 at the output of the gate.
   (e) The voltage range for a logic 1 at the output of the gate.
   (f) The voltage range for a logic 0 at the input of the gate.
   (g) The voltage range for a logic 1 at the input of the gate.
   (h) The gate delay for the low-to-high transition of the output.

3. Draw the circuit diagram for the following logic function (i.e. Boolean expression)

   \[ F(A,B,C) = A'.B.C + A.B.C' + A'.B'.C \]

   *Note: use only 3 inverters in your diagram.*

4. Draw the circuit diagram for the following logic function

   \[ F(A,B,C) = (A + B' + C').(A' + B' + C).(A' + B + C ') \]

   *Note: use only 3 inverters in your diagram.*
5. For the following circuit diagram

(a) Derive the logic function (i.e. Boolean expression)
(b) Draw the wiring diagram

*Note: when drawing the wiring diagram, use the template provided on the class webpage.*
6. For the following circuit diagram

(a) Derive the logic function
(b) Draw the wiring diagram

Note: when drawing the wiring diagram, use the template provided on the class webpage.