1. For the 74LS00, specify the following

(a) The logic operation.
(b) The truth table.
(c) The “absolute maximum” supply voltage.
(d) The voltage range for a logic 0 at the output of the gate.
(e) The voltage range for a logic 1 at the output of the gate.
(f) The voltage range for a logic 0 at the input of the gate.
(g) The voltage range for a logic 1 at the input of the gate.
(h) The gate delay for the low-to-high transition of the output.

2. For the 74HC02, specify the following

(a) The logic operation.
(b) The truth table.
(c) The “absolute maximum” supply voltage.
(d) The voltage range for a logic 0 at the output of the gate.
(e) The voltage range for a logic 1 at the output of the gate.
(f) The voltage range for a logic 0 at the input of the gate.
(g) The voltage range for a logic 1 at the input of the gate.
(h) The gate delay for the low-to-high transition of the output.

3. Draw the circuit diagram for the following logic function (i.e. Boolean expression)


*Note: use only 3 inverters in your diagram.*

4. Draw the circuit diagram for the following logic function

\[ F(A,B,C) = (A + B' + C').(A' + B' + C').(A' + B + C') \]

*Note: use only 3 inverters in your diagram.*
5. For the following circuit diagram

\[ \text{(a) Derive the logic function (i.e. Boolean expression)} \]
\[ \text{(b) Draw the wiring diagram} \]

*Note: when drawing the wiring diagram, use the template provided on the class webpage.*
6. For the following circuit diagram

(a) Derive the logic function
(b) Draw the wiring diagram

Note: when drawing the wiring diagram, use the template provided on the class webpage.
#1. The 74LS00 gate.

(a) \( F = (A \cdot B)' = \text{NAND operation} \)

(b) \[
\begin{array}{ccc}
A & B & A \cdot B & (A \cdot B)' \\
0 & 0 & 0 & 1 \\
0 & 1 & 0 & 1 \\
1 & 0 & 0 & 1 \\
1 & 1 & 1 & 0 \\
\end{array}
\]

(c) "absolute maximum" supply voltage = 7V.

(d) Voltage range for logic 0 at output

\[ \text{GND} \rightarrow V_{\text{OL}} = 0V \rightarrow 0.5V \]

(e) Voltage range for logic 1 at output

\[ V_{\text{OH}} \rightarrow V_{\text{DD}} = 2.7V \rightarrow 5V \]

(f) Voltage range for logic 0 at input

\[ \text{GND} \rightarrow V_{\text{IL}} = 0V \rightarrow 0.8V \]

(g) Voltage range for logic 1 at input

\[ V_{\text{IH}} \rightarrow V_{\text{DD}} = 2V \rightarrow 5V \]

(h) gate delay for low-to-high transition of output

\[ t_{\text{PHL}} = 3 \rightarrow 10 \text{ ns} \quad (4 \rightarrow 15 \text{ ns}) \]
#2. The 74 HC 02 gate

(a) \( F = (A+B)' = \text{NOR} \) operation.

(b) 

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>A+B</th>
<th>(A+B)'</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
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<td>0</td>
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<td>1</td>
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<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

(c) "absolute maximum" supply voltage = \( 7 \) V

(d) Voltage range for logic 0 at the output

\[ \text{GND} \rightarrow V_{OL} = 0V \rightarrow 0.26V \quad (0.1V) \]

(e) Voltage range for logic 1 at the output

\[ V_{OH} \rightarrow V_{DD} = 4.18V \rightarrow 4.5V \quad (5.68V \rightarrow 6.0V) \]

(f) Voltage range for logic 0 at the input

\[ \text{GND} \rightarrow V_{IL} = 0V \rightarrow 1.8V \quad (1.35V) \]

(g) Voltage range for logic 1 at the input

\[ V_{IH} \rightarrow V_{DD} = 3.15V \rightarrow 4.5V \quad (4.2V \rightarrow 6.0V) \]

(h) gate delay for low-to-high transition of output

\[ t_{DHL} = 9 \rightarrow 15 \text{ns} \quad (8 \rightarrow 13 \text{ns}) \]
3. \( F(A, B, C) = \overline{A}BC + ABC + \overline{A}BC \).

4. \( F(A, B, C) = (A + \overline{B} + C)(\overline{A} + \overline{B} + C)(\overline{A} + B + C) \)
$F = (A + B) \cdot (B + C) \cdot (\overline{A} + \overline{C})$
#6. $F = \overline{A} \cdot B + B \cdot \overline{C}$

$VCC$ (supply voltage)