Homework #3

due: Wednesday, February 16, 2011

1. Given the following Boolean expression (do not simplify):

   \[ F(A,B,C) = A'BC' + ABC' + A'B'C \]

   (a) Write the VHDL Entity statement for this logic circuit.

   (b) Using the “Boolean expression” model, write the VHDL Architecture statement.

   (c) Using the “Truth table” model, write the VHDL Architecture statement.

   Extra Credit:

   (d) Using the Structural model, write the VHDL Architecture statement.
2. Roth and Kinney, problem 4.7

3. Roth and Kinney, problem 4.9

4. Roth and Kinney, problem 4.10

5. Roth and Kinney, problem 4.29

6. Roth and Kinney, problem 4.32 – parts (a) and (b)

7. Roth and Kinney, problem 4.35