

ECE 331
Lecture Exercise
Testbenches

Problem

Write a testbench that generates the following input stimuli. Assume that the signals `clk`, `r` and `s` are periodical, and the signals `resetn` and `m` are non-periodical. The simulation should be able to continue indefinitely under this assumption. Do your best to minimize the amount of lines of VHDL code you write by employing VHDL instructions such as FOR LOOP, etc.

