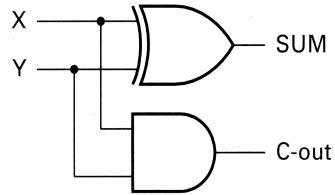
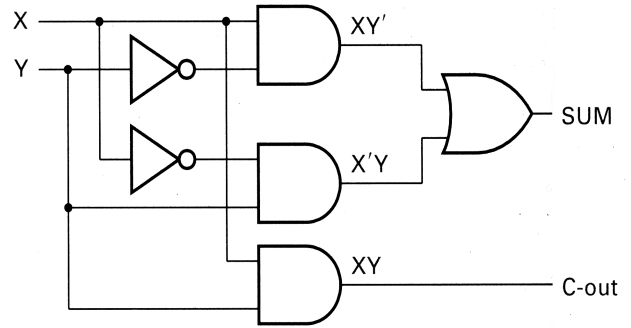


# Half Adders

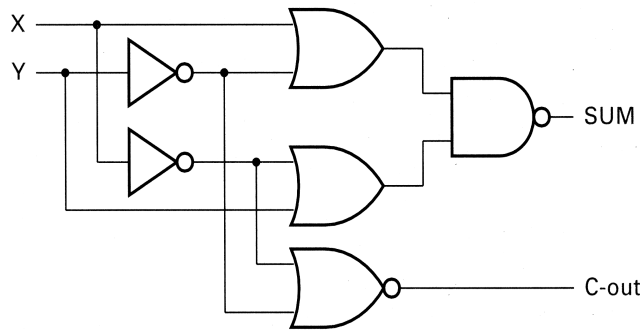
**Figure 4.47**  
Half-adder logic diagrams



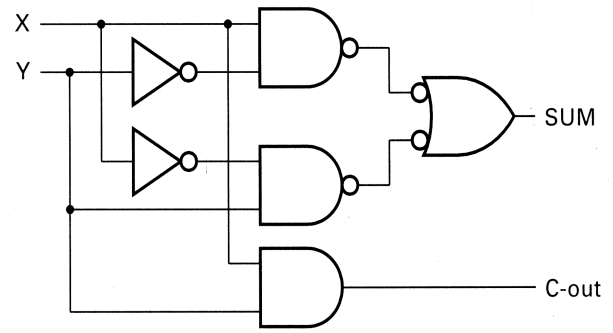
(a)



(b)



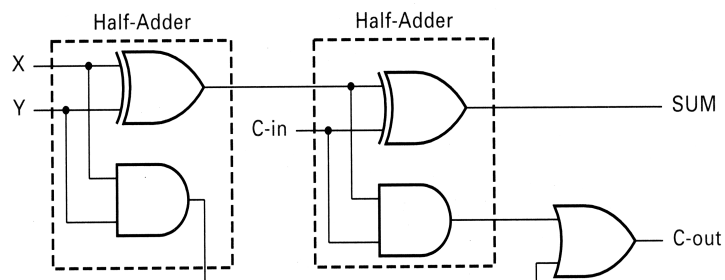
(c)



(d)

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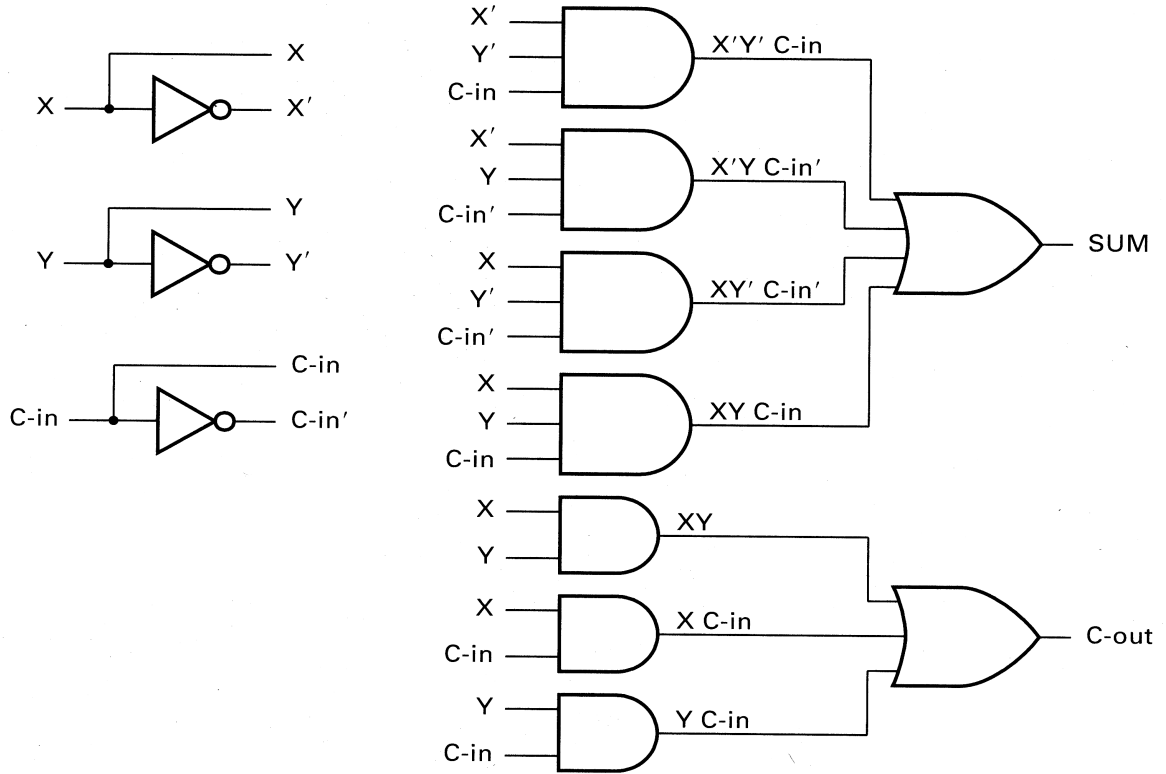
# Full Adders



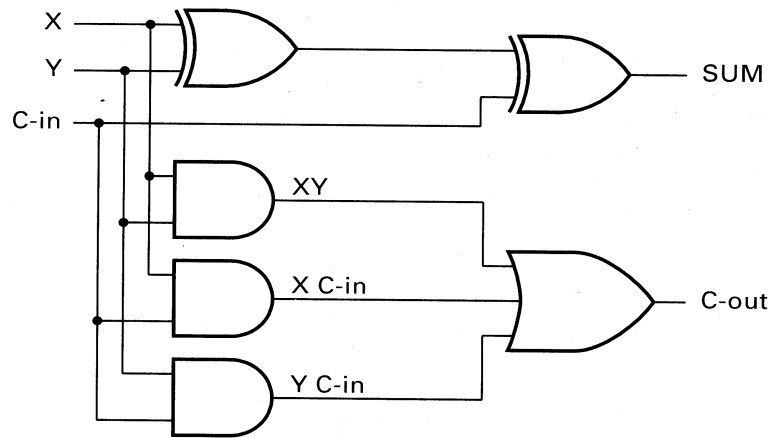
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# Full Adders (continued)

**Figure 4.49**  
Full-adder logic diagrams



**(a) Sum-of-Products**



**(b) EX-OR**