Example Final Exam

ECE331

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(The material shown might not be representative for the material covered in the actual exam. Also, the final exam will contain a multiple choice section which is not shown here. Have a look at Dr. Hintz's webpage for examples.)

- Closed book, ~~one~~ two 3"x5" note cards with **handwritten** notes allowed. Calculators permitted for basic math only (no text, etc.)
- Show all of your work. Use written English, where applicable. Always write neatly.
- A solution requiring physical units is *incorrect* if the units are omitted from the result.
- Underline, circle or box each result.

1) *(10 pts)* Determine the Boolean equation for the minimum **POS** static-hazard-free implementation of the function $F_{A,B,C,D} = \Sigma(1, 6, 9\text{–}11, 14)$. Show how you determined this implementation.

   You need **not** draw the resultant logic circuit.

2) *(10 pts)* For the pair of decimal values A and B in the table below, (*i*) express each number in the 1's complement system in columns 3 and 4, respectively, **using 8 bits** (*ii*) express each number in the 2's complement system in columns 5 and 6, respectively, **using 8 bits** and (*iii*) express their sum and difference in the 2's complement system in columns 7 and 8, respectively, **using 8 bits.**

   In all cases, write a result as "OVERFLOW" if it cannot be contained in the 8-bit representation.

Decimal Value:		**1's Comp. Number System (8 Bits)**		**2's Comp. Number System (8 Bits)**			
A	**B**	**A**	**B**	**A**	**B**	**A + B**	**A – B**
-97	30						

3) *(15 pts)* Use basic logic gates (AND, OR, NOT — any number of inputs) to **design** a **minimum SOP** combinational logic circuit to add a **two-bit** unsigned binary number (e.g. $00_2 \rightarrow 0_{10}$, $01_2 \rightarrow 1_{10}$, $10_2 \rightarrow 2_{10}$ and $11_2 \rightarrow 3_{10}$) to a **one-bit** unsigned binary number, with sufficient output bit length to contain any result.

   Your **design** should be a three-input (two bits for the two-bit unsigned integer and one bit for the one-bit unsigned integer), three-output (for the three-bit unsigned integer sum) combinational logic circuit. (Note that overflow is not possible.)

   Show your truth table, method of logic function minimization, and final logic equations for your outputs. To save time, you need **not** draw the resultant logic circuit.

use 74F00 only

4) *(15 pts)* Using only the six basic "Fast TTL" ICs listed on the exam notesheet (use the specs from this sheet as well), **implement** the function below while minimizing (*i*) maximum total power dissipated (assume V_{CC} = 5 V; and the output of each gate spends half of its time high — remember that the I_{CC} values on the notesheet are for an entire package) and (*ii*) the worst-case propagation delay.

In your design, (*i*) specify and label each part **(you must draw your circuit implementation)**, (*ii*) report the maximum total power dissipated and (*iii*) report the worst-case propagation delay.

Function: $\mathbf{F_{W,X,Y,Z} = \Sigma(3\text{–}7, 11, 15)}$.

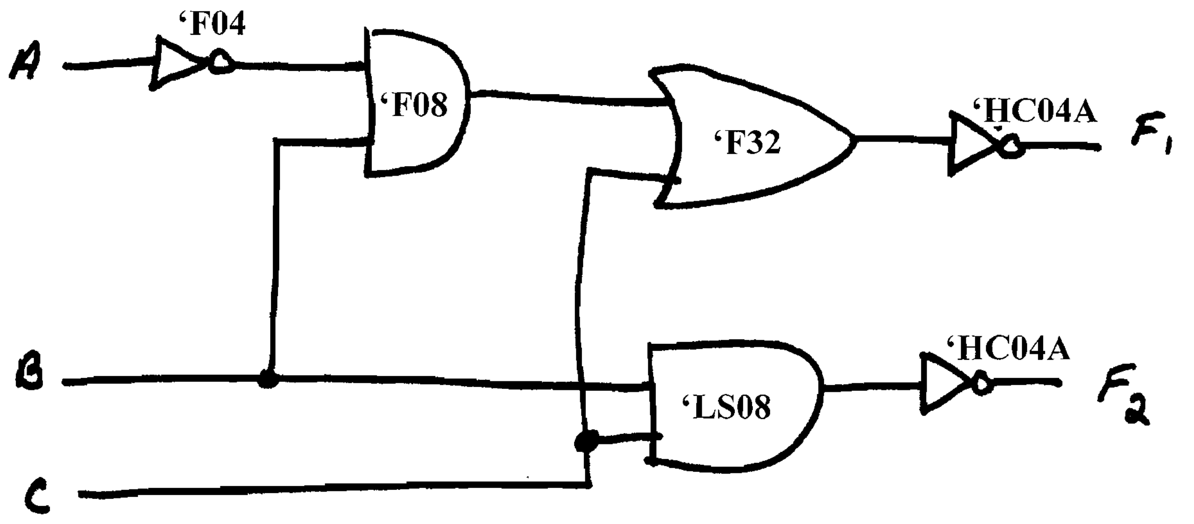
5) *(10 pts)* Determine the fanout limit when a Motorola 74HC00A NAND Gate (CMOS) drives a Motorola 74F32 OR Gate (FAST TTL).

6) *(10 pts)* For the **Motorola 74HC08A**, determine the **maximum** quiescent power dissipation, dynamic power dissipation and total power dissipation when one gate from the IC drives a capacitive load of C_L = 20 pF at a switching frequency of 10 kHz, when powered by a 5 V source. Assume the gate output spends 50% of its time in the high output state and 50% of its time in the low output state.

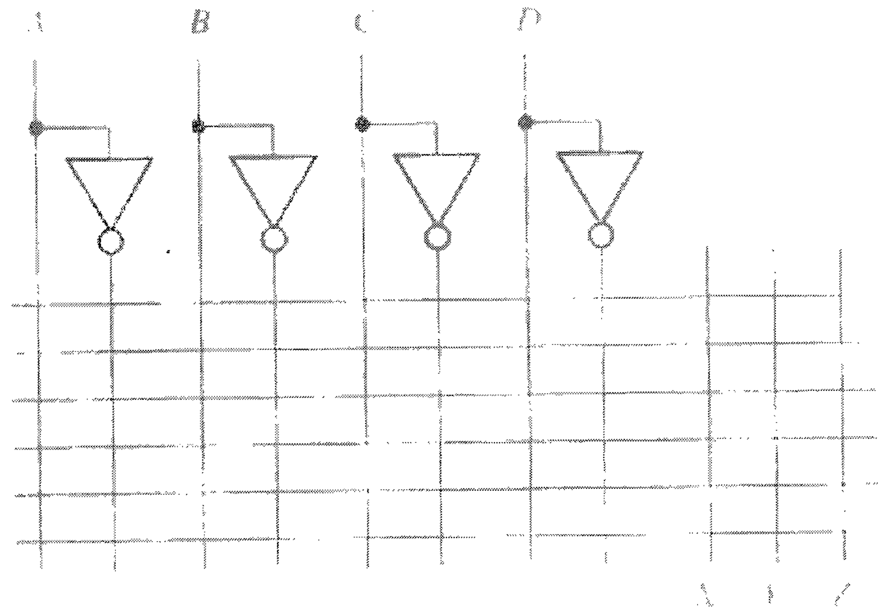
7) *(10 pts)* Use the Sum of Worst Case (SWC) analysis technique to determine the maximum propagation delay for the circuit shown below. ***Show how you determined this value.***

- For Fast TTL parts ("'Fyy"), use Motorola MC74Fyy parts.
- For LS TTL parts ("'LSxx"), use Motorola SN74LSxx parts.
- For CMOS parts ("'HCzz"), use Motorola 74HCzz parts.

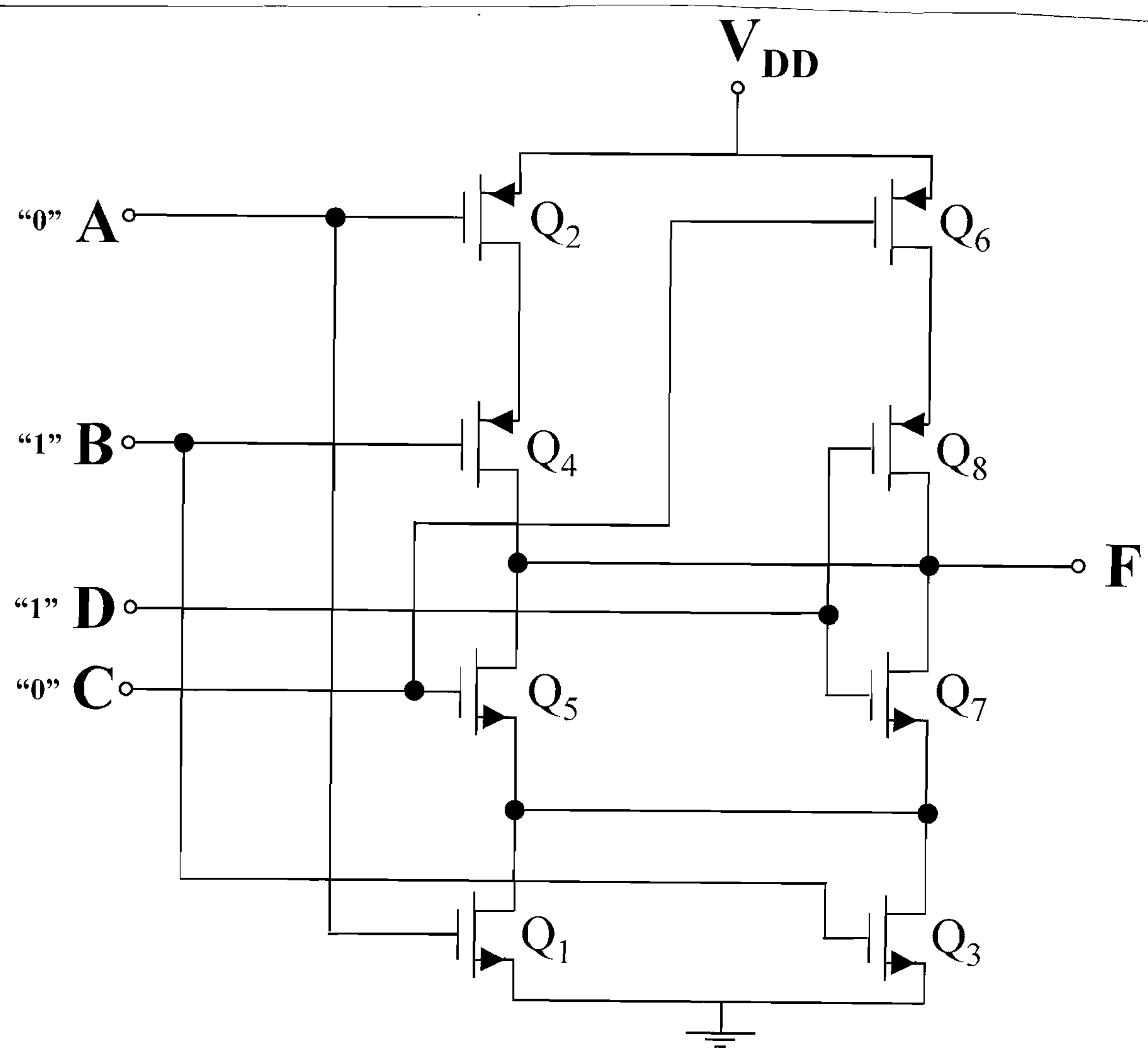
All necessary specifications should be available on your test notesheet.



8) *(10 pts)* Use the "short hand" notation for showing the programming of the PLA below to implement: $X_{A,B,C,D} = \Sigma(3, 6, 11, 15)$.



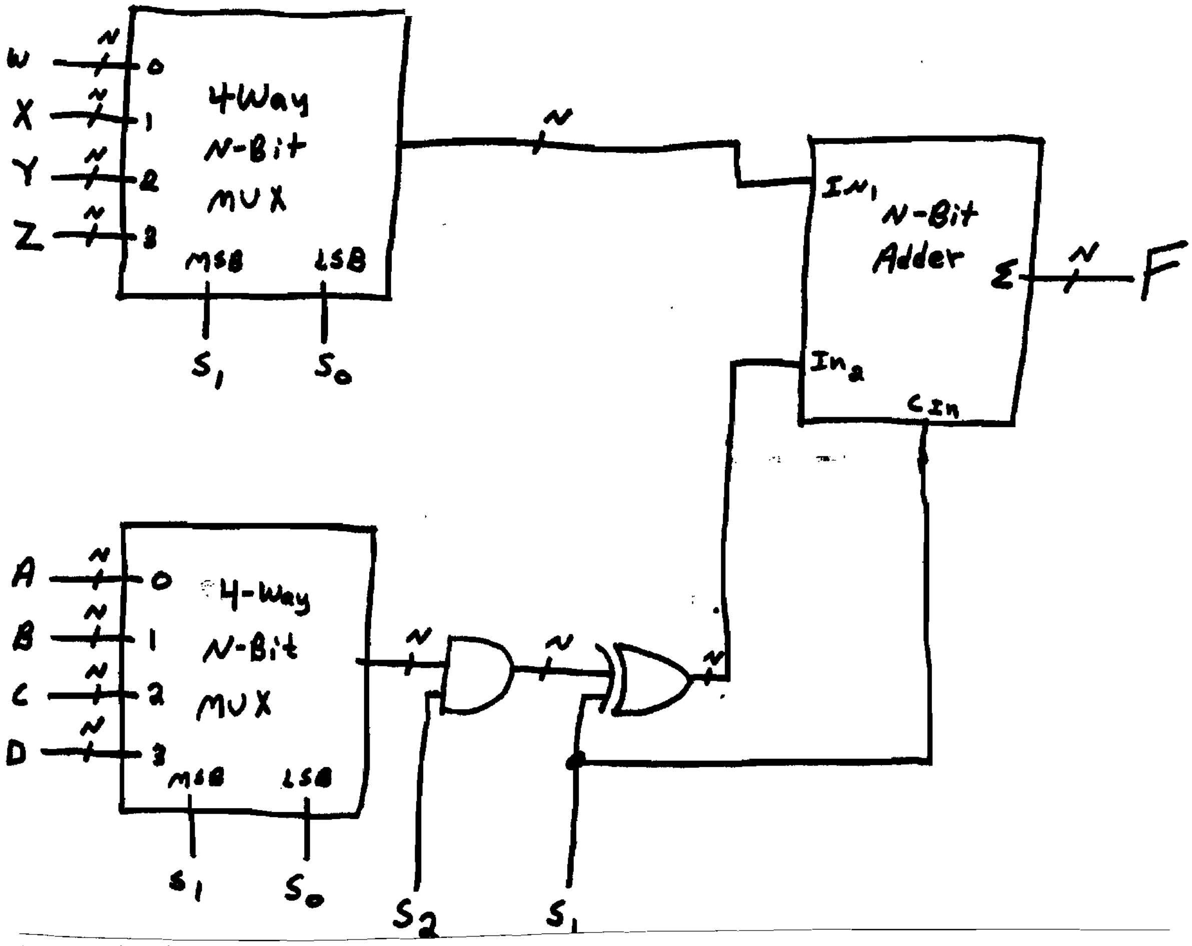
9) *(15 pts)* Determine the ON/OFF state of each transistor (Q1 through Q8) and the logic value of the output in the CMOS circuit shown below when: A = 0, B = 1, C = 0, and D = 1 (logic levels).



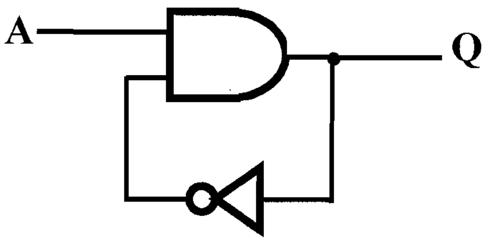
10) *(15 pts)* The ALU below has N-bit 2's complement data inputs W, X, Y, Z, A, B, C and D; control input bits S_0, S_1 and S_2; and an N-bit data output F. The XOR and AND gates each represent N gates (one per bit), respectively.

Determine the arithmetic function performed by this ALU for each of the eight possible control inputs shown in the Instruction Code table.

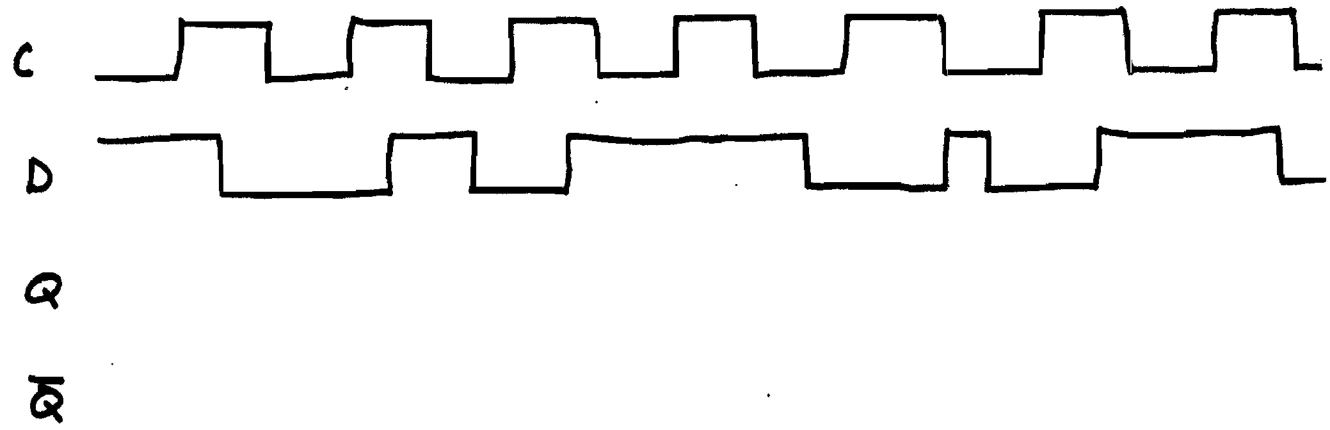
Instruction Code $S_2\ S_1\ S_0$	Function F = ?
0 0 0	
0 0 1	
0 1 0	
0 1 1	
1 0 0	
1 0 1	
1 1 0	
1 1 1	



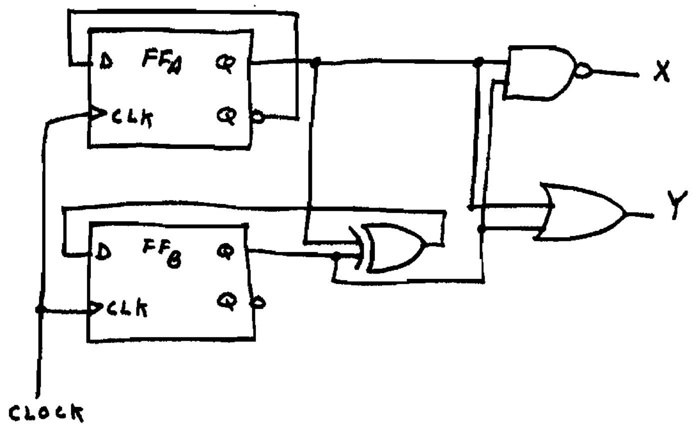
11) *(10 pts)* The circuit below (with input "A" and output "Q") utilizes feedback. Describe, in words (written English!), the operation of the circuit separately for the cases when A = 0 (logic low) and A = 1 (logic high).



12) *(10 pts)* The figure below shows a partial timing diagram. Draw the corresponding timing diagrams for the two resulting output waveforms Q and Q', if C and D are the inputs to an **edge-triggered D flip-flop**.

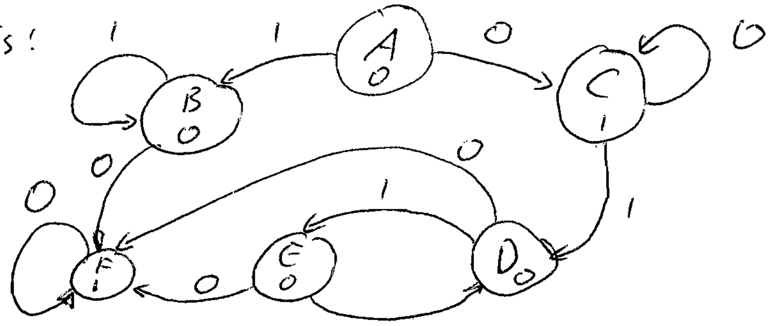


13) *(15 pts)* Analyze the sequencer shown below using the four-step process to *i*) Identify the next state and output logic, *ii*) Write the output and next state equations, *iii*) Construct the Transition Table and *iv*) Construct the State Transition Diagram.



14) Design a State Machine of type Mealy that detects the sequence "1101". Use JK Flip-Flops.

15) Minimize this!



Which sequence does it detect?