

Experiment 0 — OR3 Gate

ECE 332 — Section 000

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June 8, 2003

On my honor I have neither received nor given aid on this report.

Signed: *Ronald J. Hayne*

Part I

Description of the Experiment

Experiment 0 was designed to use a simple example to demonstrate the use of the Mentor Graphics software, ModelSim.

A 3-input OR function is implemented, such that the output is true if any of the 3 inputs are true. The algebraic expression for the 3-input OR function is:

$$Z = A + B + C$$

The truth table of the function is shown below:

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

In order to simulate the propagation delay evident in a hardware implementation of such a gate, it has been specified that the output signal should change value (if applicable) 10ns after a change in an input signal.

Part II

Software Implementation

The VHDL code used to model the example circuit is presented in this section, along with the testbench used to test the circuit by driving the input signals through their full range of values.

or3.vhd

```
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-- Author           : Dr. Ron Hayne
-- Date            : April 13, 2003
-- Course          : ECE332
-- File Name       : or3.vhd
-- Design Units    : OR3
-- Purpose of Code : This is an example circuit provided for
--                 : the Mentor Graphics Tutorial.
-- Hardware modeled : Behavioral model of a 3-input OR gate.
-- Model Limits     : None known
-- Known Errors     : None known
-- Design Library   : work
-- Dependencies     : None
-- Environment:
--   Simulator      : Mentor Graphics (ModelSim) V5.4d
--   Platform       : Unix (SunOS 5.8)
-- Change List (most recent on top)
--   Date    Who   What
--   ----- ---   ----
--   07Jun03 rjh   Update to ESA coding stds
--   13Apr03 rjh   Creation
-----

library IEEE;
use IEEE.std_logic_1164.all;

entity OR3 is
  port( A : in std_logic;
        B : in std_logic;
        C : in std_logic;
        Z : out std_logic );
end OR3;
-----

architecture BEHAVE of OR3 is
begin

  Z <= A or B or C after 10 ns;

end BEHAVE;
```

or3_testbench.vhd

```

-----
-- Author           : Dr. Ron Hayne
-- Date            : May 26, 2003
-- Course          : ECE332
-- File Name       : or3_testbench.vhd
-- Design Units    : OR3_Testbench
-- Purpose of Code : This is a top level testbench for the OR3
--                  example which is provided for the Mentor
--                  Graphics Tutorial.
-- Hardware modeled : This testbench creates an instance of the
--                  OR3 circuit and then drives the inputs
--                  and checks the results.
-- Model Limits    : VHDL-93 Syntax (report)
-- Known Errors    : None known
-- Design Library  : work
-- Dependencies    : OR3
-- Environment:
--   Simulator     : Mentor Graphics (ModelSim) V5.4d
--   Platform      : Unix (SunOS 5.8)
--
-- Change List (most recent on top)
--   Date      Who   What
--   -----   ---   ----
--   07Jun03  rjh   Update to ESA coding stds
--   26May03  rjh   Creation
-----

library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity OR3_Testbench is
end OR3_Testbench;

architecture Testbench of OR3_Testbench is
    signal Input: std_logic_vector(2 downto 0) := "000";
    signal Z : std_logic;

    component OR3
        port( A : in std_logic;
              B : in std_logic;
              C : in std_logic;
              Z : out std_logic );
    end component;

```

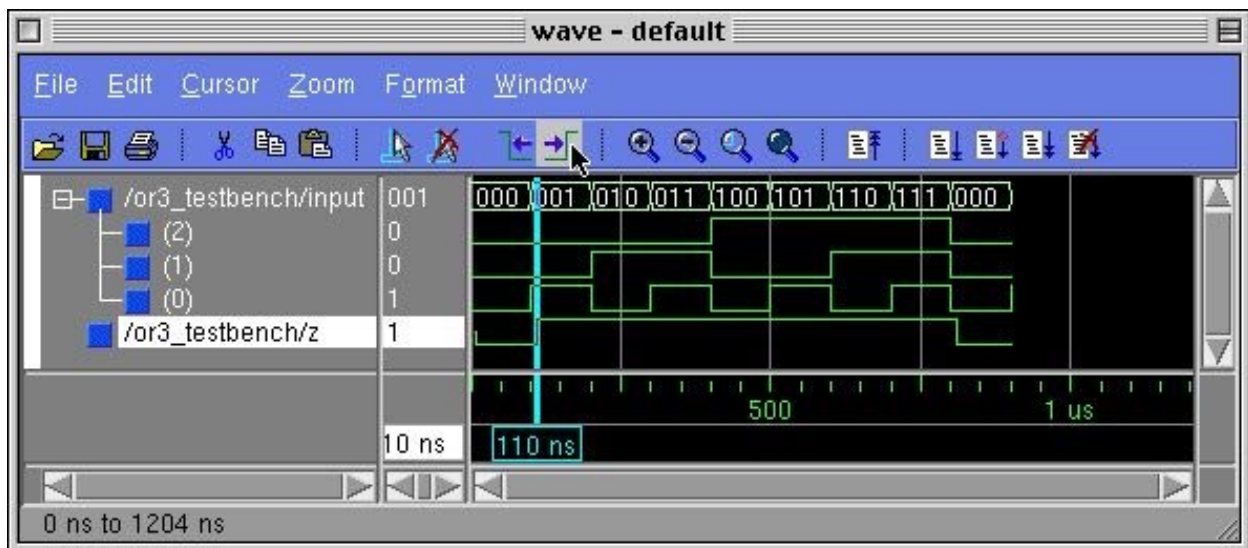
```

begin
  -- Component Instantiation
  Tested_Circuit : OR3 port map( A => Input(2),
                                B => Input(1),
                                C => Input(0),
                                Z => Z );

  -- Cycle through test vectors and evaluate the results
  process
  begin
    wait for 100 ns;
    case Input is
      when "000" =>
        assert (Z = '0')
          report "Test Failed";
      when others =>
        assert (Z = '1')
          report "Test Failed";
    end case;
    Input <= Input + "001";
  end process;
end Testbench;

```

The VHDL code for the OR3 function and its corresponding testbench were compiled and simulated using ModelSim. The resulting waveforms are shown below:



From the timing diagram of the simulation results the proper implementation of the OR3 function is verified by the output Z being a 1 whenever any of the inputs (A,B,C) is a 1. The correct modeling of the propagation delay is shown by the cursor position at 110ns. The output Z changes from a 0 to a 1 10ns after the input C changes from a 0 to a 1.

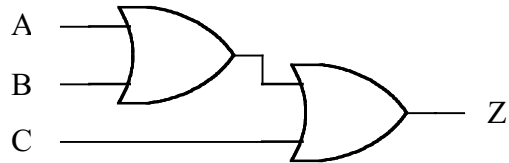
Part III

Hardware Implementation

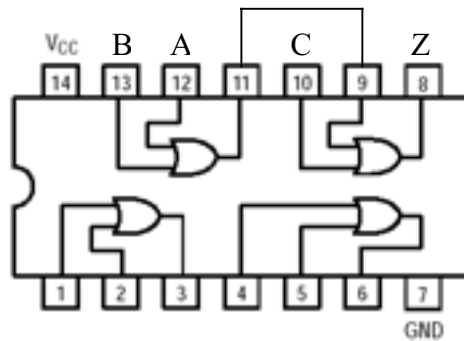
The following IC chips were used to implement this circuit:

(1) 74LS32 Quad 2 Input OR Gate

The logic diagram is show below:



The hardware wiring diagram is shown below:



The hardware implementation was constructed and tested using the wiring diagram shown above. The test results replicated the truth table shown in Part I, verifying the proper operation of the circuit.

Part IV

Conclusion

Both hardware and software implementations of the OR3 function were studied in this experiment. While both implementations produced the same logical results, the propagation delays were different due to variable delay paths introduced in the hardware implementation, due to the cascading of multiple 2-input OR gates to produce the 3-input OR function.