**Ideal Inverter**

Voltage Transfer Characteristic (VTC) of the ideal inverter
Generic Inverter VTC

Voltage Transfer Characteristic (VTC) of a typical inverter
Noise Margins

Propagation of digital signals under the influence of noise
Noise Margins

Definition of noise margins

\[ NM_L = V_{IL} - V_{OL} \]
\[ NM_H = V_{OH} - V_{IH} \]
Noise Margins

Nominal output

\[ V_{\text{out}} = f(V_{\text{in}}) \quad (5.5) \]

Output under noise

\[ V'_{\text{out}} = f(V_{\text{in}} + \Delta V_{\text{noise}}) \quad (5.6) \]

\[ V'_{\text{out}} = f(V_{\text{in}}) + \frac{dV_{\text{out}}}{dV_{\text{in}}} \cdot \Delta V_{\text{noise}} + \text{higher order terms (neglected)} \quad (5.7) \]

The nominal operating region is defined as the region where the gain is less than unity!

Perturbed Output = Nominal Output + Gain × External Perturbation \quad (5.8)
CMOS Inverter Circuit
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\[ V_{\text{out}} = V_{\text{in}} - V_{T0,p} \]

\[ V_{\text{out}} = V_{\text{in}} - V_{T0,n} \]

- nMOS in saturation
- pMOS in saturation
- both in saturation

Input Voltage (V)

Output Voltage (V)

\[ V_{T0,p} \]

\[ 0 \]

\[ V_{T0,n} \]

\[ V_{IL} \]

\[ V_{IH} \]

\[ V_{DD} + V_{T0,p} \]

\[ V_{DD} \]
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\[ V_{IL} = \frac{2V_{OUT} + V_{T0,P} - V_{DD} + k_R V_{T0,N}}{1 + k_R} \]  
\[ V_{IH} = \frac{V_{DD} + V_{T0,P} + k_R \cdot (2V_{OUT} + V_{T0,N})}{1 + k_R} \]

\[ V_{th} = \frac{V_{T0,N} + \sqrt{\frac{T}{k_R}} \cdot (V_{DD} + V_{T0,P})}{1 + \sqrt{\frac{T}{k_R}}} \]
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nMOS transistor current-voltage characteristics
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pMOS transistor current-voltage characteristics
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Intersection of current-voltage surfaces of nMOS and pMOS transistors
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Intersection of current-voltage surfaces gives the VTC in the voltage plane
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- $V_{DD} = 5\, V$
- $V_{T0,n} = 1.0\, V$
- $V_{T0,p} = -1.0\, V$
- $k_n = k_p$

Output Voltage (V) vs. Input Voltage (V)

- Drain Current vs. Drain Current ($10^{-5}\, A$)

- VTC
- $V_{th}$

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How to choose the $k_R$ ratio to achieve a desired inversion threshold voltage:

$$k_R = \frac{k_n}{k_p} = \left( \frac{V_{DD} + V_{T0,p} - V_{th}}{V_{th} - V_{T0,n}} \right)^2$$

(5.73)

$$\frac{k_n}{k_p} = \frac{\mu_n \cdot C_{ox} \cdot \left( \frac{W}{L} \right)_n}{\mu_p \cdot C_{ox} \cdot \left( \frac{W}{L} \right)_p} = \frac{\mu_n \cdot \left( \frac{W}{L} \right)_n}{\mu_p \cdot \left( \frac{W}{L} \right)_p}$$

(5.77)
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- $V_{DD} = 5\, \text{V}$
- $V_{T0,n} = 1.0\, \text{V}$
- $V_{T0,p} = -1.0\, \text{V}$

Output Voltage (V) vs. Input Voltage (V) graph with different values of $k_R$:
- $k_R = 0.25$
- $k_R = 1.0$
- $k_R = 4.0$
Supply Voltage Scaling

VTC of a CMOS inverter for different power supply voltage values.

\[ V_{T0,n} = 1.0 \text{ V} \]
\[ V_{T0,p} = -1.0 \text{ V} \]

\[ V_{DD} = 5.0 \text{ V} \]
\[ V_{DD} = 4.0 \text{ V} \]
\[ V_{DD} = 3.3 \text{ V} \]
\[ V_{DD} = 2.0 \text{ V} \text{ (limit case)} \]
\[ = V_{T0,n} + |V_{T0,p}| \]
Supply Voltage Scaling

VTC of a CMOS inverter, when operated with a supply voltage that is smaller than \((V_{Tn} + |V_{Tp}|)\).

→ Hysteresis behavior!
CMOS Inverter Layout
CMOS Inverter Layout

Mask layout of the inverter

Simplified cross-section