ECE680: Physical VLSI Design

Examples of Timing Issues in IC

Example 1

\[ \begin{align*}
I & \rightarrow D \rightarrow Q \\
& \quad \text{CLK} \\
& \quad \text{CL}_1 \quad 80\text{ns} \\
& \quad b \\
& \quad \text{CLK} \\
& \quad \text{CL}_2 \quad 30\text{ns} \\
& \quad d \\
& \quad \text{CLK} \\
& \quad e \\
\end{align*} \]
Example 2

Consider the following latch based pipeline circuit shown in Figure 0.8.

Assume that the input, \( IN \), is valid (i.e., set up) 2ns before the falling edge of \( CLK \) and is held till the falling edge of \( CLK \) (there is no guarantee on the value of \( IN \) at other times). Determine the maximum positive and negative skew on \( CLK' \) for correct functionality.

**Latch Parameters:**
- \( t_{D-Q} = 1\text{ns} \) (\( D \) to \( Q \) delay)
- \( t_{\text{hold}} = 0 \)
- \( t_{su} = 1\text{ns} \)

\[ t_{\text{in, su}} = 2\text{ns} \]

\[ T = 20\text{ns} \]
What is the maximum positive and negative skew on CLK’?
Assume the propagation through NAND gate can be 5 ns, 10 ns or 20 ns with equal probability. The second logic stage is always ready for the data from the first stages.

Use synchronous clock to replace HS

\[
\begin{align*}
    t_{HS} &= 6 \text{ ns} \\
    t_p &= \frac{5 + 10 + 20}{3} + 6 = 17.67 \text{ ns}
\end{align*}
\]

\[
\begin{align*}
    t_{HS} &= 12 \text{ ns} \\
    t_p &= \frac{5 + 10 + 20}{3} + 12 = 23.67 \text{ ns}
\end{align*}
\]

\[
\begin{align*}
    f &= \frac{1}{20 \text{ ns}} = 50 \text{ MHz} \\
    f &= \frac{56.6}{\text{MHz}} \\
    f &= 42.2 \text{ MHz}
\end{align*}
\]