1. Your name:

2. The recent study regarding the comparison of the area, speed, and power of ASICs vs. FPGAs, reported in the paper assigned to you as your required reading, was performed at
   a. MIT
   b. GMU
   c. GWU
   d. University of Toronto
   e. Carnegie Melon University
   f. UCLA
   g. Stanford

3. An average ratio of the FPGA vs. ASIC dynamic power consumption for two circuits performing the same function (assuming the use of logic only in FPGAs) is equal to approximately:
   a. 2  b. 7  c. 12  d. 40  e. 100

4. List at least three advantages of FPGAs when compared to ASICs?

5. List at least three features of Handel-C that make this language different from ANSI-C and suitable for describing hardware:
6. List the names of at least three companies specializing in the development of design automation toolsets for FPGAs:

7. List four primary inputs and one primary output of the Synopsys Design Compiler:

Inputs:

Output:

8. The name of the Synopsys tool used for the placing and routing of ASICs is:

9. What is a difference between an abstract view and a layout view of an ASIC library cell?

10. Connection between two metal layers in ASICs is called:
11. The single Block RAM sizes in Spartan 3 and Virtex 5 are equal to:

Spartan 3:

Virtex 5:

12. What is the name of the two most recent families of Altera FPGA devices in each of the following categories:

low-cost:

high-performance:

13. What is the name of the building block of Xilinx FPGAs that enables the fast execution of additions, subtractions, and comparisons?

14. List at least two functions of a clock manager in Xilinx FPGAs:

15. The difference between SelectMAP and ICAP reconfiguration interfaces used in Virtex II FPGAs is that:
16. FPGAs based on the following configuration technologies are instantly on after power-up, without requiring any configuration (multiple answers may be correct):

a. antifuse  
b. SRAM  
c. EEPROM  
d. FLASH  
e. Fusible-link

17. Single Event Upset (SEU) is the name of a random soft error caused by …………….. 

18. Which of the following constructs of VHDL are non-synthesizable (more than one answer may be correct)?

- initializations (e.g., SIGNAL a : STD_LOGIC := ‘0’;)
- for-generate
- multiplication of real numbers
- selected concurrent signal assignment (with-select-when)
- delays (e.g. a <= b after 10 ns;)

19. True or false? (give an answer separately for each statement)

a. All inputs to the combinational circuit described using a process in VHDL should be included in the sensitivity list
b. All inputs to the sequential circuit described using a process in VHDL should be included in the sensitivity list

20. What is wrong about the following architecture of a combinational comparator? How would you correct this code?

ARCHITECTURE Behavior OF comparator IS  
BEGIN
    PROCESS ( A, B )
    BEGIN
        IF A = B THEN
            AeqB <= '1';
        END IF;
        END PROCESS;
END Behavior ;
21. Group the following four objects in VHDL into two pairs of objects with similar properties (the objects within the same pair may be used in the same places in your code):
   a. constants
   b. signals
   c. ports
   d. generics

22. What is the name of the microprocessor embedded in the Xilinx Virtex 4 FX FPGAs?

23. Physical verification of a placed and routed ASIC includes the following three checks (give abbreviations and full names):

24. List at least two vendors of Reconfigurable Supercomputers:

25. List at least three high level languages other than C, C++, or Java that can be used to describe reconfigurable hardware:

26. What are the characteristic features of the following Xilinx Virtex 4 subfamilies:
   Virtex-4 LX:
   Virtex-4 SX:
   Virtex-4 FX:
27. List at least three **numerical** differences between Virtex 5 and Virtex 4 FPGA devices (i.e., it is not sufficient to say that one device is faster than the other, you need to provide maximum clock frequencies for both):

28. The name of the fast serial interconnect capable of reaching speeds in access of 10 Gbit/s for communication between two FPGAs is:

29. The two primary differences between PCI-X and PCI are (give numerical values describing these differences):

30. Two primary bus sizes and the two corresponding clock frequencies used in PCI are:

   **Bus sizes:**

   **Clock frequencies:**