Problem 1 (2.5 points)

For a given below VHDL code, provide solutions to the following problems:

1. Which type of a finite state machine, Moore or Mealy, does this code implement?
2. Draw an ASM chart describing this FSM. Assume that all inputs and outputs are active with logic one.
3. Supplement timing waveforms given in the answer sheet with values of state_next, state_reg and output tick.

```vhdl
library ieee;
use ieee.std_logic_1164.all;

entity edge_detect is
  port(
    clk, reset: in std_logic;
    level: in std_logic;
    tick: out std_logic
  );
end edge_detect;

architecture behavioral of edge_detect is
  type state_type is (zero, edge, one);
  signal state_reg, state_next: state_type;
begin
  -- state register
  process(clk,reset)
  begin
    if (reset='1') then
      state_reg <= zero;
    elsif (clk'event and clk='1') then
      state_reg <= state_next;
    end if;
  end process;

  -- next-state/output logic
  process(state_reg,level)
  begin
    state_next <= state_reg;
    tick <= '0';
    case state_reg is
      when zero=>
        if level= '1' then
          state_next <= edge;
        end if;
      when edge=>
        if level= '0' then
          state_next <= zero;
        end if;
      when one=>
        if level= '0' then
          state_next <= zero;
        end if;
    end case;
  end process;
end behavioral;
```
when edge =>
    tick <= '1';
    if level= '1' then
        state_next <= one;
    else
        state_next <= zero;
    end if;
when one =>
    if level= '0' then
        state_next <= zero;
    end if;
end case;
end process;
end behavioral;

Problem 2 (2.5 points)

Write a testbench that is able to comprehensively test 8-bit barrel shifter with the following entity declaration:

entity barrel_shifter is
    port(
        a:  in std_logic_vector(7 downto 0);
        amt: in std_logic_vector(2 downto 0);
        y:   out std_logic_vector(7 downto 0)
    );
end barrel_shifter ;

This particular barrel shifter is defined as a circuit that rotates 8-bit input a to the right by the number of positions specified as a value of the input amt.

The testbench should allow the generation of an output y corresponding to each possible combination of values of inputs a and amt.
Problem 3 (2.5 points)

a. Write an architecture describing the given below circuit, called EXAM_1, in synthesizable VHDL. Assume that the reset inputs of the D flip-flop and the counter are synchronous, and active high, and the values of \( k \) and \( DD \) are provided as generics.

b. Write a statement instantiating the described component with the values of generics \( k=8 \) and \( DD=200 \), and the names of signals connected to the respective inputs and outputs provided in the interface diagram below.
Problem 4 (2.5 points)

What is a minimum number of Spartan 3 Logic Cells (one Logic Cell = ½ of a CLB Slice) necessary to implement

a. Functions \( y_1 = x_1x_2 + x_2x_3 + x_1x_4x_5 \), \( y_2 = x_1x_2 + x_4 + x_5 \)

b. 32-bit unsigned comparator (A>B)

c. 48-bit shift register with serial input, serial output, and reset

d. Full Adder

e. 24-bit shift register with serial input, serial output, and enable

f. 8-input priority encoder

g. 64x32 single-port RAM

h. 32x8 dual-port RAM

Which components of Logic Cells (Multipurpose LUT, Carry & Control, Storage Element) are used in each case, and in which mode of operation (ROM, RAM, shift-register, fast carry logic, latch, flip-flop, etc.) they work?