Problem 3

a) Registers R0-R2:
   32 Logic Cells, each cell implements a 3-stage shift register using
   1 MLUT operating in the Shift Register mode.

Register R3:
   32 Logic Cells, each cell implements a 1-bit register using
   1 Storage Element operating in the Flip-Flop mode.

b) 16-bit adder:
   16 Logic Cells, each cell implements one stage of a ripple carry adder (Full Adder) using
   1 Carry & Control logic + 1 MLUT in the ROM (logic) mode.

c) 16-bit subtractor:
   16 Logic Cells, each cell implements one stage of a ripple carry subtractor using
   1 Carry & Control logic + 1 MLUT in the ROM (logic) mode.

d) 16-bit comparator:
   16 Logic Cells, each cell implements one stage of a ripple carry subtractor
   (used for comparison), using
   1 Carry & Control logic + 1 MLUT in the ROM (logic) mode.

Total number of Logic Cells = 2 \cdot 32 + 3 \cdot 16 = 64 + 48 = 112

Total number of MLUTs = 32 + 3 \cdot 16 = 32 + 48 = 80.