Resource Utilization after Synthesis:

- Number of Slices: 15 out of 960 (1%)
- Number of Slice Flip Flops: 17 out of 1920 (0%)
- Number of 4 input LUTs: 29 out of 1920 (1%)
- Number of IOs: 19
- Number of bonded IOBs: 19 out of 83 (22%)
- Number of GCLKs: 1 out of 24 (4%)

Resource Utilization after Implementation:

- Number of External IOBs: 19 out of 83 (22%)
- Number of External Input IOBs: 11
- Number of External Input IBUFs: 11
- Number of External Output IOBs: 8
- Number of External Output IOBs: 8
- Number of External Bidir IOBs: 0
- Number of BUFGMUXs: 1 out of 24 (4%)
- Number of Slices: 18 out of 960 (1%)
- Number of SLICEMs: 0 out of 480 (0%)

Timing and Critical path from Static timing analysis after PAR:

Timing summary after Synthesis:
Minimum period: 4.709ns (Maximum Frequency: 212.359MHz)

Timing summary after Implementation:
Minimum period: 4.002ns\{1\} (Maximum frequency: 249.875MHz)

Timing constraint: Default period analysis for net "clk_BUFGP"
116 paths analyzed, 58 endpoints analyzed, 0 failing endpoints
0 timing errors detected. (0 setup errors, 0 hold errors)
Minimum period is 4.002ns.

Maximum Data Path: Top_module/Shift_Ph/qt_0 to Top_module/Shift_E/qt
Location               Delay type  Delay(ns)  Physical Resource  Logical Resource(s)
| SLICE_X2Y33.XQ   | Teko    | 0.592 | Top_module/Shift_Ph/qt<0> |
| SLICE_X2Y32.G3  | net (fanout=5) | 0.496 | Top_module/Shift_Ph/qt<0> |
| SLICE_X2Y32.Y   | Tilo    | 0.759 | Top_module/N01            |
| SLICE_X2Y32.F4  | net (fanout=1) | 0.023 | Top_module/Madd_Adder_out_xor<3>111_SW0 |
| SLICE_X2Y32.X   | Tilo    | 0.759 | Top_module/N01            |
| SLICE_X0Y31.F1  | net (fanout=3) | 0.481 | Top_module/N01            |
| SLICE_X0Y31.CLK | Tfck    | 0.892 | Top_module/Shift_E/qt     |
|                 |         |       | Top_module/Shift_E/qt_mux0000 |
|                 |         |       | Top_module/Shift_E/qt     |

Total 4.002ns (3.002ns logic, 1.000ns route)

(75.0% logic, 25.0% route)