ECE 448

Midterm Exam

March 4, 2013

HONOR CODE PLEDGE: “On my honor I have neither given nor received aid on this exam”

Your first and last name (printed):  ………………………

Your signature  ………………………

Failure to sign the pledge may result in receiving no credit for the exam.
Problem 1 - ASM chart

Dataflow VHDL code for the output function computing p, r, and y, as a function of the state S, and the inputs a and b:
Problem 2 – Block Diagram of Combinational Logic
library ...........;
use ................................;

entity misr is

........................................ (C : std_logic_vector(7 downto 0 ));
port ( 
    -- inputs
    clk : in std_logic;
    rst : in std_logic;
    en : in std_logic;
    D : in std_logic_vector (7 downto 0 );

    -- outputs
    Q_out: out std_logic_vector (7 downto 0 )
);
end misr;

architecture mixed of misr is

-- intermediate signals
signal  Q : std_logic_vector (7 downto 0); 
signal  Q0_replicated : std_logic_vector (7 downto 0); 
signal  d_ff_in : std_logic_vector (7 downto 0); 

begin 

    Q0_replicated <= ........................................;
    d_ff_in <= D xor ('0' & .................................) xor (C and ......................);

    -- D flip flop operation
    D_FFs: process (............................)
    begin
        if (................. = '1') then
            Q <= ......................;
        elsif ......................... then
            if(en = '1') then
                Q <= ......................
            end if;
        end if;
    end process;

    Q_out <= ..............................;
end mixed;
Problem 4 – FPGA Resources
Problem 5 – Simple Testbench